40V, 600mA Low Dropout Linear Regulator

Description

- SL9451 is a high-frequency (1.8MHz) step-down switching regulator with an integrated high-side high-voltage power MOSFET. It provides up to 0.6A of efficient output in a single channel, achieving rapid loop response through current mode control.
- With a wide input voltage range from 4.2V to 40V, it is suitable for various buck power conversion applications in mobile environment inputs. Its shutdown static current of 1uA makes it ideal for battery-powered applications.
- Under light load conditions, efficiency in a wide load range is achieved by reducing switching frequency to minimize switch and gate driver losses.
- Frequency fold back technology helps prevent inductor current runaway during startup. Thermal shutdown ensures reliable and fault-tolerant operation. The circuit package is SOT23-6L.

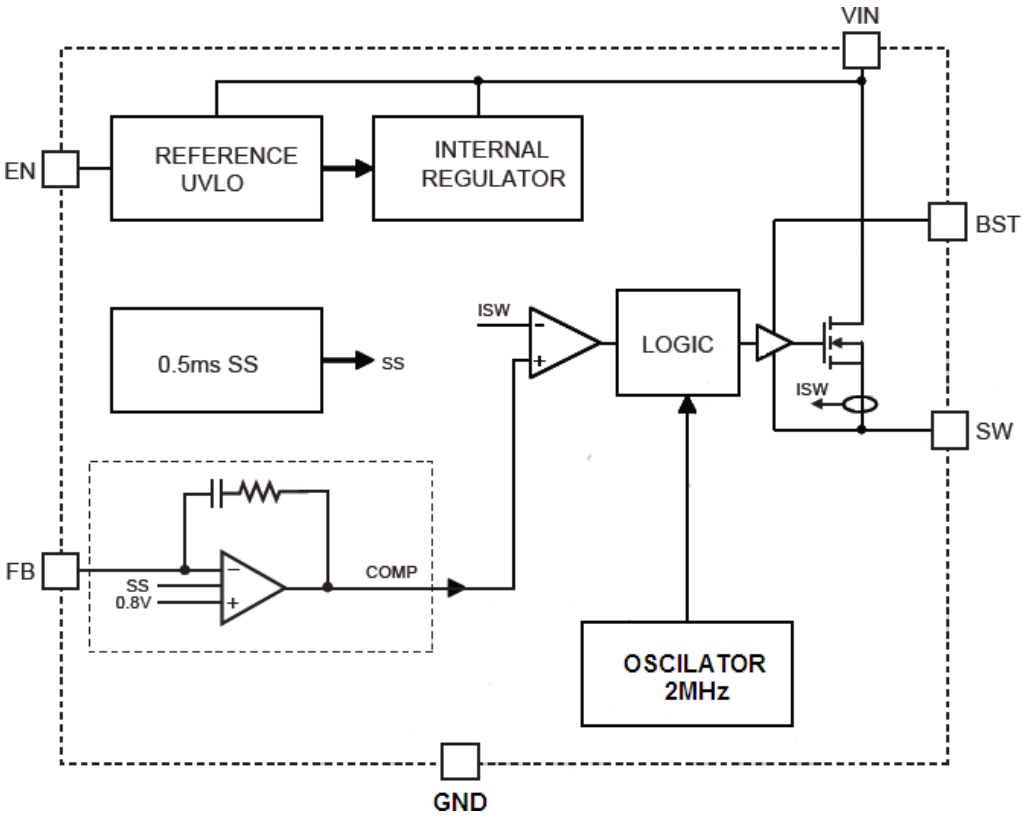
Features

- 230uA operating quiescent current
- Wide operating voltage range from 4.2V to 40V
- Internal power MOSFET with 500mΩ on-resistance
- Fixed switching frequency of 1.8 MHz
- Internal compensation
- Ceramic output capacitor for stability
- Internal soft-start
- Precision current limit without sampling resistor
- Up to 90% efficiency
- Low shutdown current: <1uA
- 6-pin SOT23 package

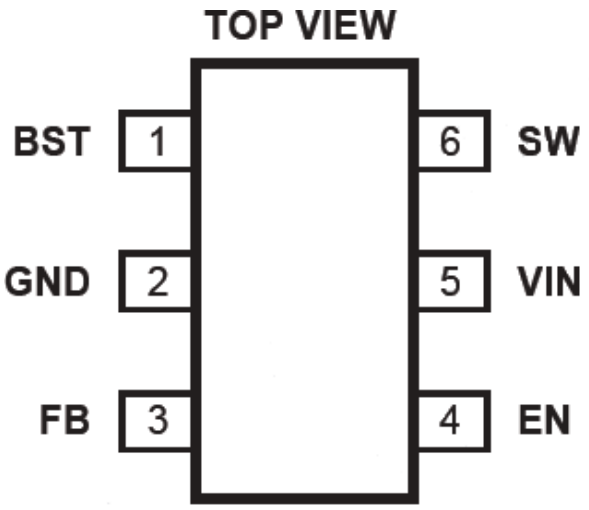
Application

- High voltage power conversion
- Automotive systems
- Industrial power systems
- Distributed power systems
- Battery-powered systems

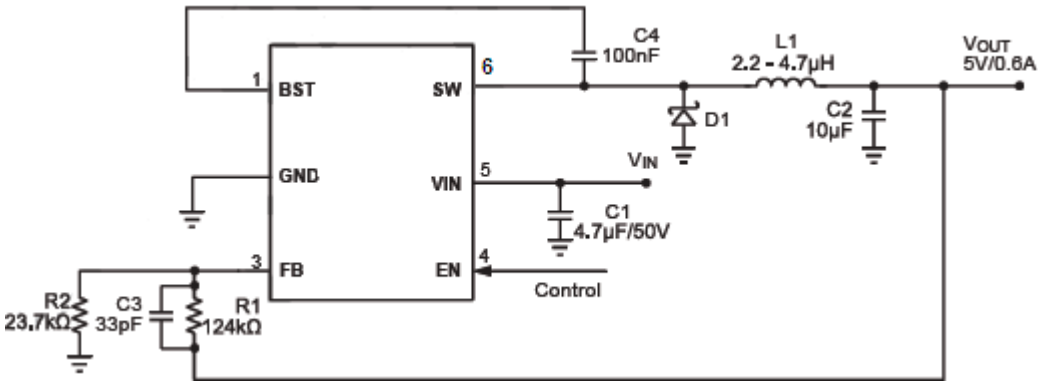
Block diagram



Outline diagram



Application diagram



Maximum ratings

Parameter	Value
supply voltage(VIN)	-0.3V to 43V
switch voltage (VSW)	-0.3V to VIN (max)+0.3V
BST to SW	-0.3 to 6.0V
other pins	-0.3V to 5.0V
continuous power consumption (TA=+25°C)	0.57W
node temperature	150°C
pin temperature	260°C
storage temperature	-65°C to 150°C

Recommended working conditions

Parameter	Value
supply voltage V_{IN}	4.2V to 40V
sw terminal voltage V_{OUT}	Up to 40V
junction temperature (T_J)	-40°C to +125°C

Thermal resistance

	θ_{JA}	θ_{JC}	
SOT23-6L	220	110	°C/W

Electrical parameter

Vin=12V, Ven=2V, Ta=25°C,except for special conditions.

Symbol	Parameter	Test Condictions	Min	Typ	Max	Unit
V_{fb}	feedback voltage		0.778	0.794	0.81	V
R_{sw}	switch-on resistance	V_{bst}-V_{sw}=5V		500		mΩ
I_{swleak}	switch leakage current	V_{en}=0V, V_{sw}=0V		0.1	1	uA
I_{lim}	extreme current			1		A
Gcs	transconductance	COMP to SENSE		3		A/V
V_{in} min	minimum operating voltage		4.2			V
V_{in}(uvlo)	undervoltage threshold		3.3		4.2	V
V_{in}(uvlo)hys	pressure fluctuation			0.8		V
T_{ss}	soft-start time	FB ranging 0 to 1.8V		0.5		msec
F_{osc}	frequency		1.4	1.8	2.2	MHz
T_{on} min	min switch on time			100		ns
I_{sd}	shutdown power supply current	V_{en}<0.3V		3	15	uA
I_{sq}	static current	V_{fb}=0.9V，no-load		200		uA
T_{emp}	thermal shutdown			150		°C
V_{enh}	En high level		1.6		2.0	V
En h_{ys}	En return difference			0.6		V
En V_{clamp}	En clamping voltage			7.5		V

Pin function

Number	Name	Function
1	BST	bootstrap.the positive power supply pole of the internal floating high edge mosfet driver transistor. connect the foot to sw connect a bypass capacitor.
2	GND	ground pin. connect it as close as possible to the output capacitor, away from high-current switching paths.
3	FB	feedback. the input of the error amplifier. an external resistor divider connected between the output and ground compares with an internal +0.8v reference to set the regulated voltage.
4	EN	enable input. pulling this pin voltage below the specified threshold will disable the chip. pulling it above the specified threshold enables the chip to operate. leaving the pin floating disables the chip.
5	VIN	power supply input. powers all internal control circuits, including the switching transistor. a decoupling capacitor to ground is required to reduce switching noise spikes.
6	SW	switching pin. this is the high-side switch output. a low vf schottky diode should be placed close to ground to minimize switching spikes.

Principle of operation

SL9451 is a 1.8 MHz oscillation frequency, asynchronous, step-down switching regulator circuit with an integrated high-side high-voltage power MOSFET internally.

It utilizes current mode control, providing efficient output of up to 0.6A with internal compensation. It features a wide input voltage range, internal soft-start control, and precision current limiting. Its very low static operating current makes it suitable for battery-powered applications.

Pwm controlling

Under medium to high output current conditions, the circuit operates in a mode where the output voltage is regulated through fixed frequency and peak current control. The PWM period is generated by an internal clock. The power MOSFET remains on until its current reaches the set COMP voltage.

When the power transistor is off, it stays off for at least 100 ns before the next cycle begins. Within a PWM cycle, if the current in the MOSFET does not reach the COMP set current value, the power MOSFET remains open, saving a switching operation.

Pulse skipping mode

During light load conditions, the circuit enters pulse-skipping mode to improve efficiency. Pulse- skipping is determined by its internal COMP voltage. If the COMP terminal drops below the internal sleep threshold, a pause command is generated to prevent opening clock pulses, thereby preventing the power MOSFET from opening as instructed, saving driver and switching losses. This pause command also places the entire chip into sleep mode, consuming very low static current to further enhance light load efficiency.

When the COMP voltage exceeds the sleep threshold, the pause signal resets, and the chip returns to normal PWM operation. Each time the pause command changes state from low to high, an immediate open signal is generated to turn on the power MOSFET.

Error amplifier

The error amplifier consists of an internal operational amplifier with a resistor-capacitor feedback network connected between its output (internal COMP node) and negative input (FB). When FB drops below its internal reference voltage (REF), the COMP output is driven higher by the op-amp, resulting in higher peak current output for the switch, thereby transferring more energy to the output, and vice versa.

Usually, FB is connected to a divider formed by RUP and RDN, where RDN connects FB to ground, and RUP connects the voltage output node to FB. Additionally, RUP, together with the internal compensation RC network, controls the gain of the error amplifier.

Internal voltage regulator

Most of the internal circuits are powered by an internal 2.6V regulator. This regulator is powered by VIN and operates across the full VIN range. When VIN is greater than 4.0V, the regulator outputs normally. If VIN is lower, the output decreases accordingly.

Enable control

The circuit features a dedicated enable control pin, EN. When VIN is sufficiently high, the chip can be enabled or disabled via the EN pin. It operates with active high logic. The threshold lower limit is 1.6V with a hysteresis of 0.6V. When left floating, the EN pin is internally pulled to ground, disabling the chip. When EN is pulled to 0V, the chip enters the lowest shutdown current mode. If EN is above zero but below its threshold, the chip remains in shutdown mode with slightly increased shutdown current.

Undervoltage lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating under insufficient power supply voltage conditions.

Internal soft start

Soft-start is implemented to prevent overshoot of the converter output voltage during startup. When the chip initializes, internal circuits generate a soft-start voltage (SS) that starts from 0V and ramps up slowly over a time set by the soft-start period.

If SS is below the internal reference voltage (REF), SS dominates, and the error amplifier uses SS instead of REF as its reference. When SS exceeds REF, REF takes precedence. SS is also associated with FB (feedback). SS can be significantly lower than FB but should only be slightly higher than FB. If FB unexpectedly drops, SS tracks the drop in FB, designed to handle short-circuit recovery scenarios. Upon short-circuit removal, the gradual rise of SS acts like a re-initiated soft-start process, preventing output voltage overshoot.

Thermal shutdown

Thermal shutdown is implemented to prevent the chip from overheating and malfunctioning. When the chip's temperature exceeds its upper threshold, the entire chip is shut down. Once the temperature drops below the lower threshold, thermal shutdown is cleared, allowing the chip to resume operation.

Floating driver and bootstrap charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. It has its own UVLO protection with an approximately 2.9V turn-on threshold and a 300mV hysteresis. During UVLO, the SS voltage resets to zero. When UVLO is removed, the controller initiates a soft-start process.

The bootstrap capacitor is charged and maintained at around 5V by an internal bootstrap regulator. When the voltage between BST and SW drops below the regulator's set value, a PMOS switch connects VIN to BST, allowing charging current to flow from VIN to BST and then to SW. The external circuit should provide sufficient voltage headroom to facilitate charging.

The bootstrap capacitor can charge as long as VIN is sufficiently higher than SW. When the power MOSFET is on, VIN is approximately equal to SW, so the bootstrap capacitor cannot charge. The optimal period for charging occurs when the voltage difference between VIN and SW is maximized, typically when the external freewheeling diode is conducting and SW is close to the output voltage VOUT. This happens when there is no current flowing through the inductor.

During operation at higher duty cycles, the charging time of the bootstrap capacitor decreases, potentially impairing effective charging. If the external circuit does not provide adequate voltage and time for bootstrap capacitor charging, additional external circuitry can be used to ensure proper bootstrap voltage within operational limits.The UVLO of the floating driver is not communicated to the controller. The driver's DC quiescent current is approximately 20 uA, necessitating that the supply current at the SW terminal be higher than this value to maintain normal operation.

Current comparator and current limiting

The power MOSFET current is accurately sampled through a current-sensing MOSFET and then fed into a high-speed current comparator for current mode control. This sampled current serves as one of the inputs to the current comparator. When the power MOSFET turns on, the comparator initially goes through a blanking period to avoid noise, after which it switches on. The comparator compares the sensed current with the COMP voltage. When the sampled current exceeds the COMP voltage, the comparator outputs low, which turns off the power MOSFET.The maximum current of the internal power MOSFET is limited internally on a per- cycle basis.

Startup and shutdown

When both VIN and EN are above their respective thresholds, the chip initiates its operation. The reference power section starts first, generating stable reference voltage and current. Then, the internal voltage regulator activates, providing stable voltage to the rest of the circuitry. When the internal voltage reaches its upper limit, an internal timer keeps the power MOSFET off for 50us to prevent startup transients.

The internal soft-start section begins its operation next. It initially keeps the SS output low to ensure readiness of the remaining circuits, then gradually ramps up. The chip can be shut down under three conditions: EN goes low, VIN goes low, or thermal shutdown occurs.During shutdown sequencing, signal paths are blocked first to prevent any fault triggering. Subsequently, the COMP voltage and internal supply voltage decrease. The floating driver is not governed by this shutdown command, but its charging path is disabled.

Application

Component Selection and Output Voltage Setting

The output voltage is set by the voltage divider connected to the FB terminal, according to the feedback divider ratio:
VFB = VOUT*R2/(R1 + R2)

The feedback resistor R1, along with internal compensation capacitors, sets the feedback loop bandwidth. Choosing R1 around 124KΩ achieves optimal transient response.

Inductor (L)

During input switch voltage, the inductor provides continuous current to the output load, reducing output ripple with larger values. However, this increases size, series resistance, and lowers saturation current. Typically, choose an inductor where peak current is 30% of maximum load current, ensuring it stays below the maximum switch current to prevent saturation.

Input Capacitor (C1)

The input capacitor (C1) can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, include a small ceramic capacitor (e.g., 0.1uF) placed close to the circuit to mitigate input voltage ripple. When using ceramic capacitors, ensure they have sufficient capacitance to suppress excessive input voltage ripple.

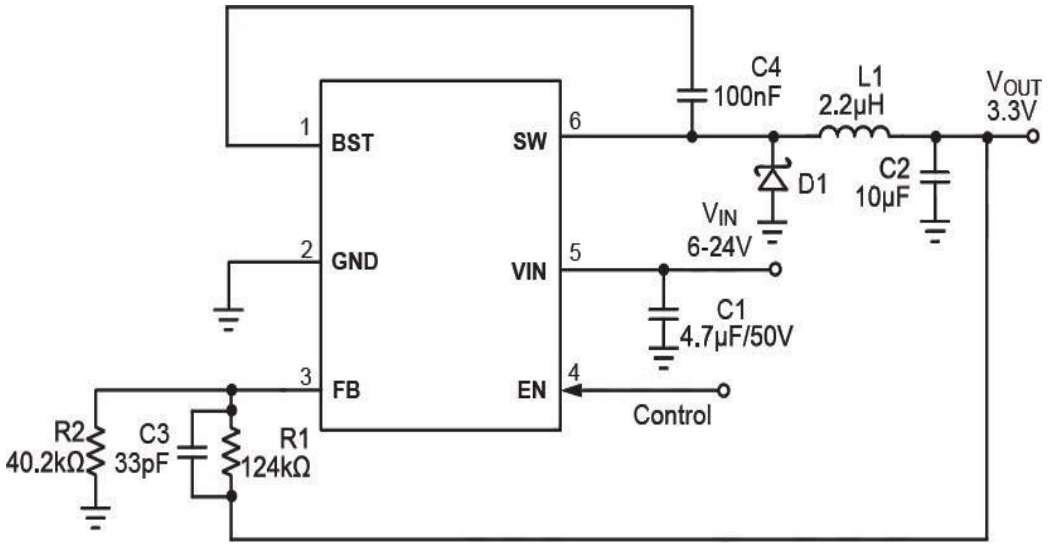
Output Capacitor (C2)

The output capacitor (C2) maintains the output DC voltage. It's recommended to use low ESR electrolytic capacitors to minimize output voltage ripple. The characteristics of the output capacitor directly influence the stability of the voltage regulation system.

Compensation Components

The design aims to optimize the converter's transfer function to achieve ideal loop gain, ensuring fast transient response and stable operation.

Typical Application Circuit



3.3V Output Application Circuit

12V Output Application Circuit

PCB Layout

The PCB layout is crucial for ensuring stable operation of the circuit. Here are some recommendations:

1) Keep the switch current paths as short as possible. Minimize the loop area formed by the input capacitor, high-side MOSFET, and external switch diode.

2) Place bypass ceramic capacitors close to the VIN terminal.

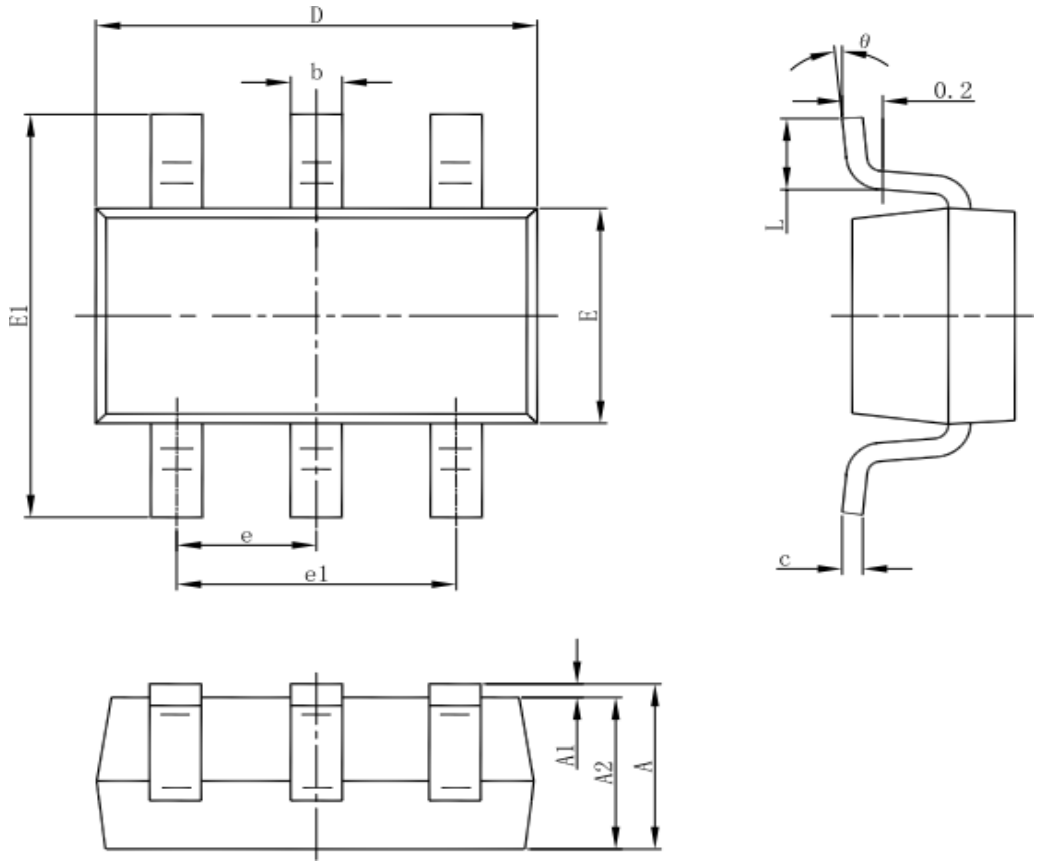
3) Ensure all connections for feedback circuits are short and direct. Position feedback resistors and compensation components as close to the chip as possible.

4) Route SW lines away from sensitive analog areas such as FB.

5) Connect SW, IN, and especially GND to large copper areas separately to enhance chip cooling, improve thermal performance, and ensure long-term reliability.

Package Dimensions Diagram:

SOT23-6L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°