11MHz Rail-to-Rail Input/Output CMOS Operational Amplifier

Description

- SL721 (single), SL722 (dual), SL723 (single with shutdown), and SL724 (quad) is a versatile operational amplifier with low noise, low voltage, and low power consumption, suitable for a wide range of applications. With an 11MHz gain-bandwidth product and 10V/μs slew rate, the S L7 21/2/3/4 are low-noise, low-voltage, low-power operational amplifiers with a power-down disable function that reduces supply current to less than 1μA. S L7 2 3 has a power-down disable function that reduces the supply current to less than 1 μA.

- Designed to provide optimum performance in low-voltage, low-noise systems, the S L7 2 1/2/3/4 offer rail-to-rail output swing for large loads, an input common-mode voltage range that includes ground, and a maximum input offset voltage of 3.5 mV. The chips can be operated over the industrial temperature range of -40°C to +125°C, and have an operating supply voltage range of 2.3 V to 5.5 V. The S L7 2 1 package type has a gain bandwidth area and conversion rate of 10 V/μs, where supply current can be reduced to less than 1 μA.

- The package types of S L7 2 1 are mainly SC70-5, SOT23-5 and SOP-8, S L7 22 are mainly SOP-8, MSOP-8, TSSOP-8 and DFN2*2-8, SL723 are mainly SOT23-6 and SOP-8, S L724 are mainly SOP-14, TSSOP-14 and QFN-16.

Feature

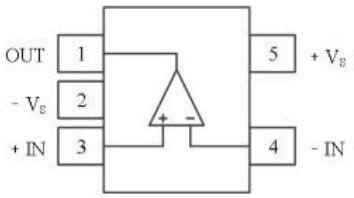
- High conversion rate: 10V/μs
- Gain bandwidth product: 11MHz
- Build-up time to 0.1%: 0.35μs
- Overload recovery time: 0.6μs
- Low noise: 12nV/ √Hz @ f=1kHz
- Input and output rail-to-rail -- Input voltage range: -0.1V to +5.6V (VS=5.5V)
- Quiescent Current: 1000μA(Typ.)
- Operating Voltage Range: +2.3V to +5.5V
- Operating Temperature Range: -40°C to +125°C

Application

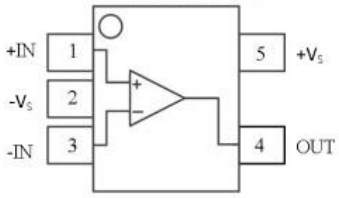
- Sensors
- Audio
- Active Filters
- A/D Converters
- Communication
- Test Equipment

Pin configuration and function

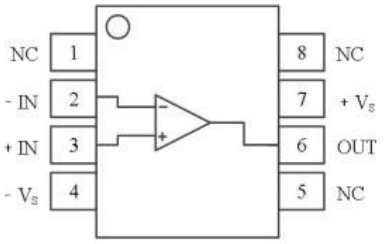
SL721
SC70-5/SOT23-5



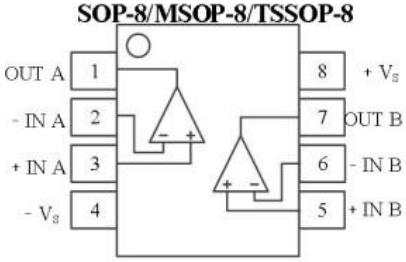
SL721U
SC70-5/SOT23-5



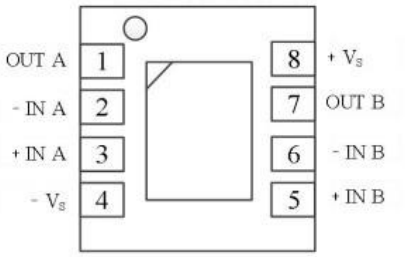
SL721
SOP-8



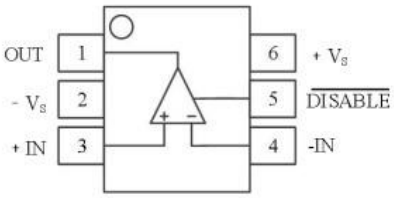
SL722
SOP-8/MSOP-8/TSSOP-8



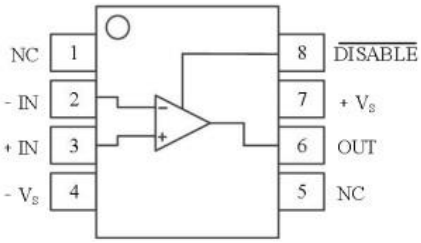
SL722
DFN-8L 2*2



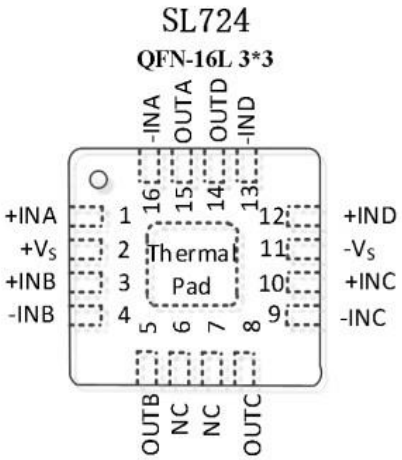
SL723
SOT23-6



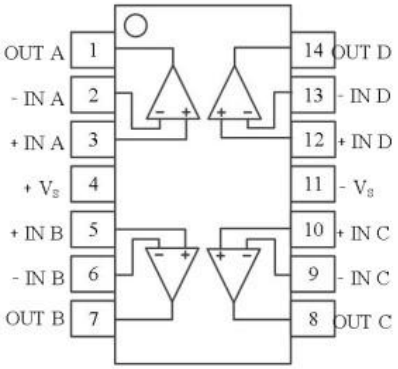
SL723
SOP-8



SL724
QFN-16L 3*3



SL724
TSSOP-14/SOP-14



Pin Arrangement

Pin function

Symbol	Description
-IN	negative (inverted) input.
+IN	positive (in-phase) input.
-INA, -INB -INC, -IND	the inverting input of the operational amplifier has an input voltage range from (VS--0.1V) to (V_S++0.1V).
+INA,+INB +INC, +IND	the in-phase input of the operational amplifier has the same input voltage range as the inverting input.
$+V_S$	positive power supply terminal with a voltage range of 2.3V to 5.5V (±1.15V to ±2.75V).
$-V_S$	negative power supply terminal, which is connected to ground in case of single power supply.
OUT	outputs.
OUTA, OUTB OUTC, OUTD	the output of the operational amplifier.
$\overline{\text{DISABLE}}$	enable terminal.
NC	no connection.

Ordering information

PN	Package	Quantity
SL721XC5	SC70-5	PEC，3000
SL721XT5	SOT23-5	PEC，3000
SL721UXC5	SC70-5	PEC，3000
SL 721UXT5	SOT23-5	PEC，3000
SL721XS8	SOP-8	PEC，4000
SL722XV8	MSOP-8	PEC，3000
SL722XS8	SOP-8	PEC，4000
SL722XT8	TSSOP-8	PEC，3000
SL722XF8	DFN-8	PEC，3000
SL723XT6	SOT-23-6	PEC，3000
SL723XS8	SOP-8	PEC，4000
SL724XS14	SOP-14	PEC，2500
SL724XT14	TSSOP-14	PEC，3000
SL724XF16	QFN-16	PEC，3000

Absolute maximum rating (T_A=25℃)

Symbol	Parameter	Value	Unit
V_S	supply voltage	±3, 6(single supply	V
V_{CM}	single input operating temperature range	V_{S-} -0.3 to V_{S+} +0.3	V
V_{DM}		±5	V
T_A	storage temperature range	-40 to 125	°C
T_{STG}	junction temperature	-65 to +150	°C
T_J	electrostatic discharge (human body model)	150	°C
ESD(HBM)	supply voltage	±8	kV

PS:
1. Exceeding the absolute maximum ratings may cause permanent damage to the device. The listed parameters are critical, and exceeding normal operating ranges for other unlisted parameters is not permissible. Prolonged operation at or near absolute maximum ratings may affect device reliability.

2. The chip must never exceed its maximum junction temperature at any time.

Electrical Parameter

（V_S = 5V, T_A = +25℃, V_{CM} = V_S/2, V_O = V_S/2, R_L = 10kΩ connect to V_S/2, Unless otherwise specified）

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Input characteristics						
V_{OS}	input offset voltage		-3.5	0.5	+3.5	mV
V_{OS} TC	input offset voltage drift	T_A=-40℃to+125℃		3		μV/℃
I_B	input bias current	V_{CM}=V_S/2		1		pA
I_{OS}	input offset current			1		pA
V_{CM}	common-mode input voltage range	T_A=-40℃to+125℃	V_{S-}–0.1		V_{S+}+0.1	V
CMRR	common-mode rejection ratio (cmrr) open-loop voltage gain input offset voltage input offset voltage drift	-0.1V<V_{CM}<3.5V	70	90		dB
		T_A=-40℃to+125℃		80		
		-0.1V<V_{CM}<5.1V	65	85		
		T_A=-40℃to+125℃		75		
A_{VOL}	input bias current	R_L=600Ω, 0.2V<V_O<4.8V	80	88		dB
		T_A=-40℃to 125℃		80		
		R_L=10kΩ, 0.1V<V_O<4.9V	90	102		
		T_A=-40℃to+125℃		90		
output characteristics						
V_{OH}	high output voltage swing low output voltage swing	R_L=600Ω		V_S–65		mV
		R_L=10kΩ		V_S–7		
V_{OL}	short-circuit output current high output voltage swing	R_L=600Ω		50		mV
		R_L=10kΩ		5		
I_{SC}	low output voltage swing	pull-up current		70		mA
		pull-down current		70		
Power supply characteristics						
V_S	operating voltage range		2.3		5.5	V
PSRR	power supply rejection ratio (psrr) quiescent current	V_S=2.7Vto 5V V_{CM}=V_S+0.5V	70	90		dB
		T_A=-40℃to+125℃		85		
I_Q	power supply current in disabled mode (only for sl723) operating voltage range	I_{OUT}=0		1000	1300	μA
		T_A=-40℃to+125℃			1700	
I_{shut}	power supply rejection ratio (psrr)			0.1	2	μA

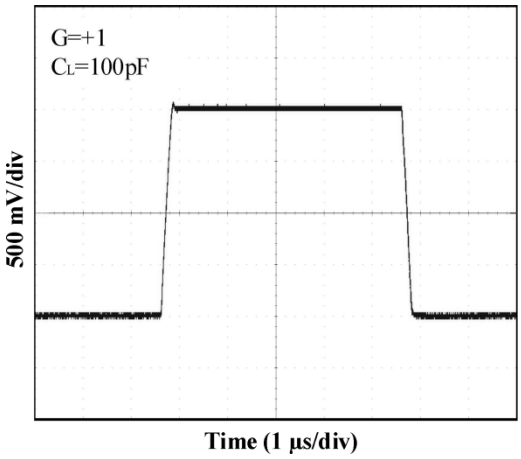
Electrical Parameter

（V_S = 5V, T_A = +25℃, V_{CM} = V_S/2, V_O = V_S/2, R_L = 10kΩ connect to V_S/2, Unless otherwise specified）

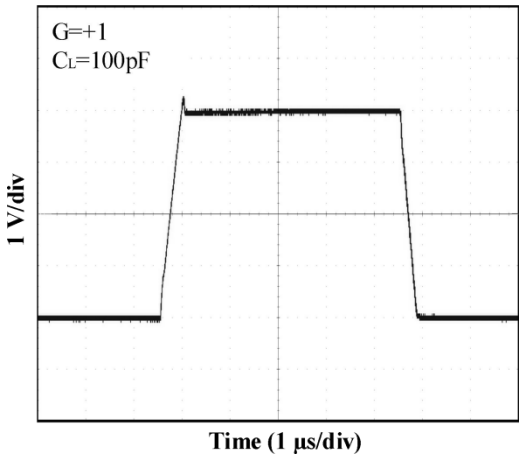
Symbol	Parameter	Condition	Min	Typ	Max	Unit
noise characteristics						
e_n	input voltage noise density	f=1kHz		12		nV/ √Hz
		f=10kHz		8		nV/ √Hz
power-off disable (sl723 only)						
	Turn-on time			1		μs
	Turn-off time			0.3		μs
	$\overline{DISABLE}$ Turn-off voltage				0.8	V
	$\overline{DISABLE}$ Turn-on voltage		2			V
dynamic characteristics						
GBP	gain-bandwidth product			11		MHz
φ_O	phase margin			60		°
SR	slew rate	G=1,2V output step		10		V/μs
t_S	settling time to 0.1%	G=1,2V output step		0.35		μs
t_{OR}	overload recovery time	V_{IN}×G=V_S		0.6		μs

Typical performance characteristics curves

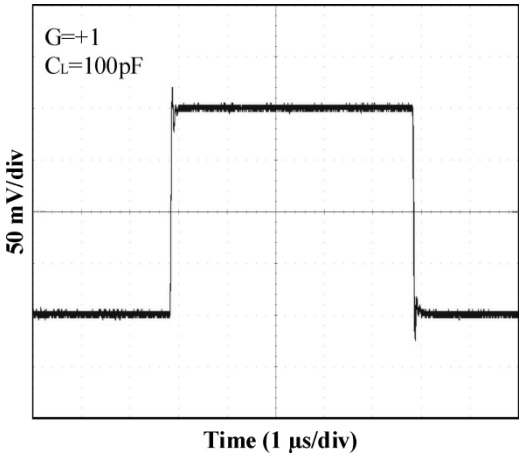
（V_S = 5V, T_A = +25℃, V_{CM} = V_S/2, V_O = V_S/2, R_L = 10kΩ connect to V_S/2, Unless otherwise specified）



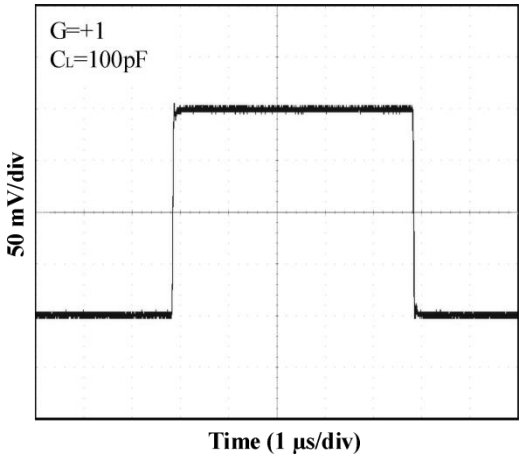
Large step response at 2.3V



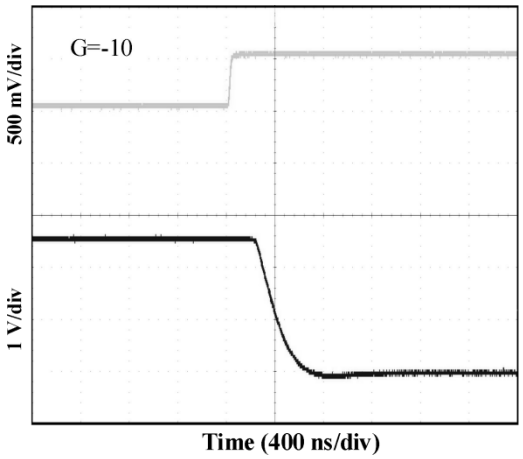
Large step response at 5V



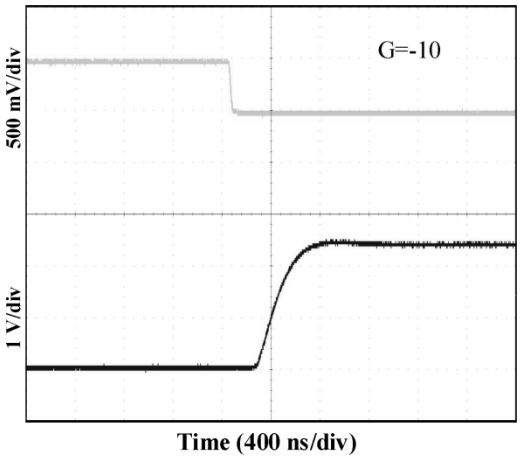
Small step response at 2.3V



Small step response at 5V



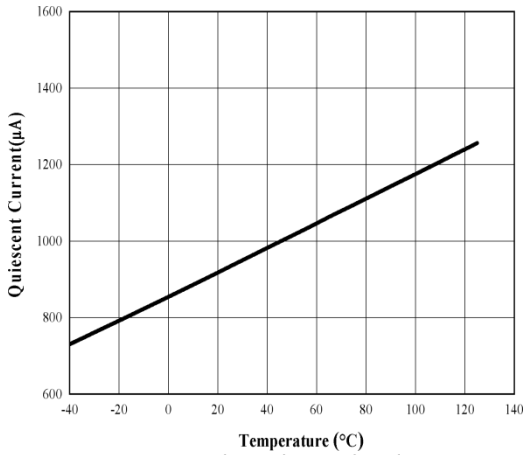
Positive overload recovery



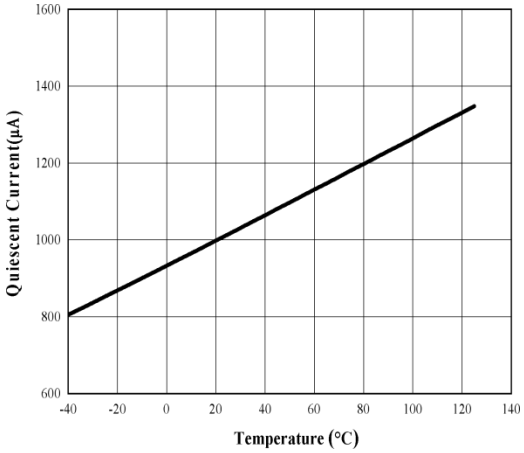
Negative overload recovery

Typical performance characteristic curves

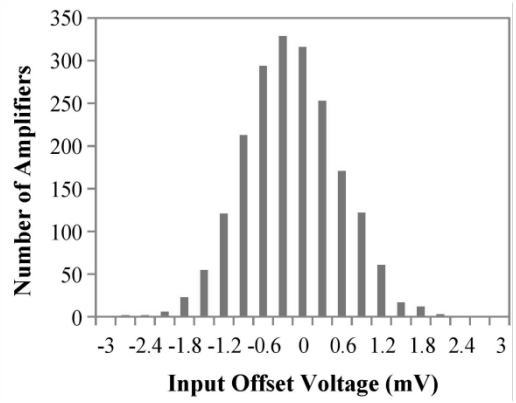
（V_S = 5V, T_A = +25℃, V_{CM} = V_S/2, V_O = V_S/2, R_L = 10kΩ connect to V_S/2, Unless otherwise specified）



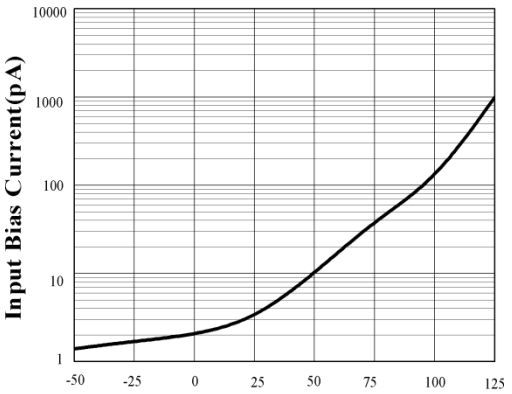
Temperature dependence of static current at 2.3V



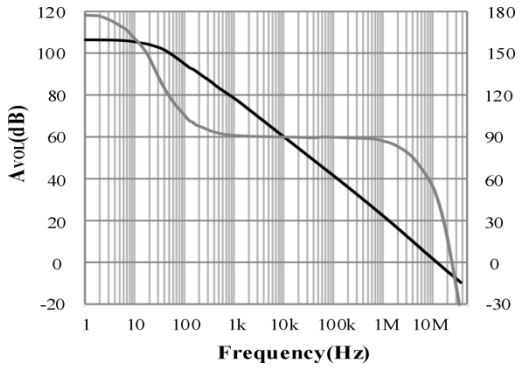
Temperature dependence of static current at 5V



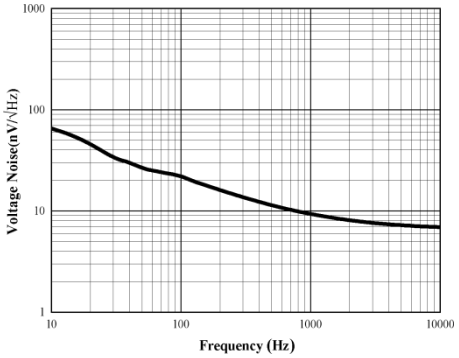
Input offset voltage drift



Temperature dependence of input bias current



Frequency response of open-loop gain and phase



Frequency dependence of input voltage noise spectral density

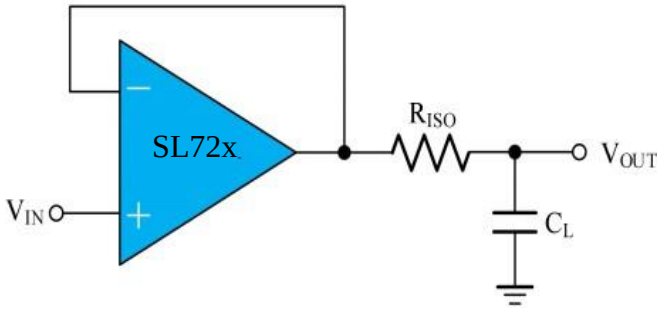
Application

1. Operating Characteristics

SL72x operates in a voltage range of 2.3V to 5.5V.The input voltage range is ±(1.15V to ±2.75V).Operating temperature range is from -40°C to +125°C. The typical characteristics exhibit parameters that significantly vary with operating voltage or temperature.

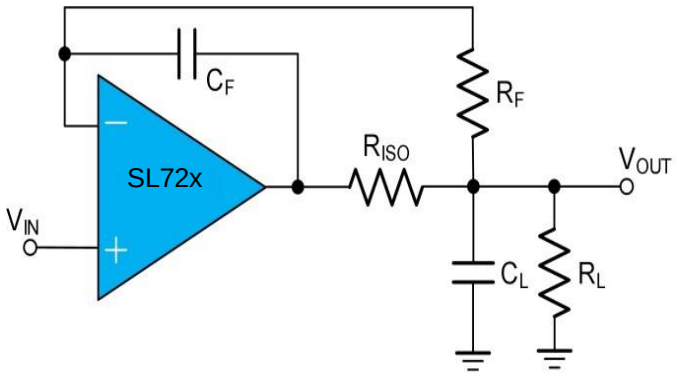
2. Capacitive Load and Stability

SL72x can guarantee stability without oscillation when directly driving a 1000pF capacitor in a unity gain configuration. The unity gain follower is most sensitive to capacitive loads, and directly driving capacitive loads reduces the amplifier's phase margin, potentially leading to ringing or oscillation. If the application requires greater capacitive drive capability, isolation resistors should be used between the output and the capacitive load, as shown in Figure 14. Isolation resistor RISO and load capacitor CL form a zero to enhance stability. A larger value of RISO increases the stability of VOUT. Note that due to RISO and RL forming a voltage divider, this approach may result in a loss of gain accuracy.



Indirectly driving large capacitive loads

Improved circuitry as shown in Figure 15 provides DC accuracy and AC stability by connecting resistor RF to the inverting signal to the output.



Indirectly driving capacitive loads enhances DC accuracy

3. Input Bias Current

The SL72x series is a CMOS operational amplifier series with extremely low pA-level input bias currents. The low input bias currents allow the amplifier to be used in applications with high impedance sources, but care must be taken to minimize PCB surface leakage.

4. Power Supply Layout and Bypassing

The operating voltage range for SL72x is +2.3V to +5.5V for single supply and ±1.15V to ±2.75V for dual supplies. For single-supply operation, ceramic capacitors (i.e., 0.01μF to 0.1μF) should be used to bypass the supply VS, and these capacitors should be placed near the VS pin (within 2mm for optimal high-frequency performance).

In dual-supply operation, 0.1μF ceramic capacitors should be used to bypass VS+ and VS- pins to ground. Larger capacitance capacitors (such as 2.2μF or larger tantalum capacitors) within 100mm should be used to provide bulk and slow current for better performance. These larger capacitors can be shared with other analog components.

The PCB layout should optimize performance by minimizing stray capacitances at the inputs and outputs of the operational amplifier. To reduce stray capacitance, external components should be placed as close to the device as possible, using surface-mount devices where feasible. It is strongly recommended to solder the operational amplifier directly to the board to minimize loop area for high-frequency and large current to reduce electromagnetic interference (EMI).

5. Grounding

In SL72x circuit design, the grounding layer is crucial. The length of the current path in the return line can induce unwanted voltage noise, and a wide grounding area reduces parasitic inductance.

6. Input-Output Coupling

To minimize capacitance coupling, input and output signal lines should not run parallel, which helps reduce unnecessary positive feedback.

7. Layout Guidelines

To achieve optimal circuit performance, the following layout principles should be followed when designing the printed circuit board (PCB):

A. External components (e.g., feedback resistors) should be placed as close to the chip as possible to minimize parasitic capacitance and the Seebeck effect.

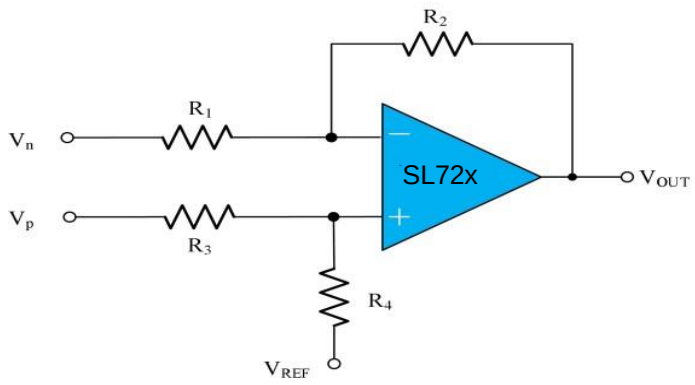
B. Input signal wires should be kept as short as possible and away from power lines or other digital signal lines.

C. Each power pin should be connected to ground with a low ESR, 0.1μF ceramic bypass capacitor as close to the chip as possible. In single-supply applications, a capacitor should connect between the power supply and ground.

D. Key routing areas may benefit from adding a low-impedance, driven guard ring, which significantly reduces leakage currents between nearby different potentials.

8. Differential Amplifier

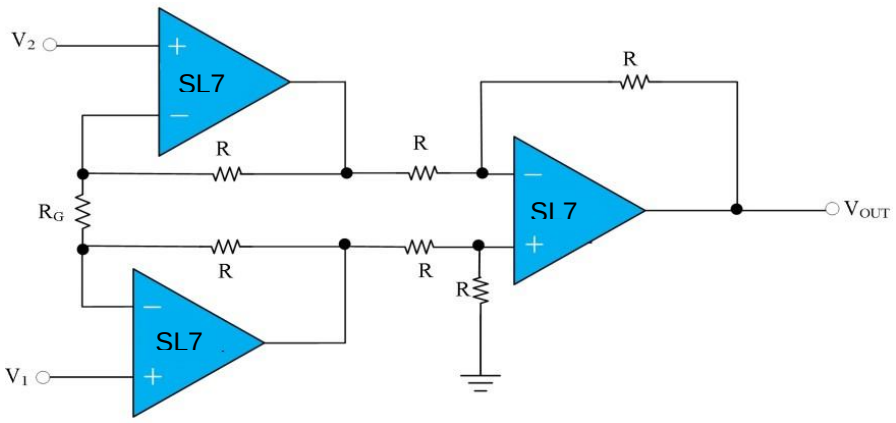
The circuit in Figure 16 is a differential amplifier circuit. If the resistor ratios are equal ($R_4/R_3 = R_2/R_1$), then $V_{OUT} = (V_p - V_n) * R_2/R_1 + V_{REF}$.



Differential Amplifier

9. Instrumentation Amplifier

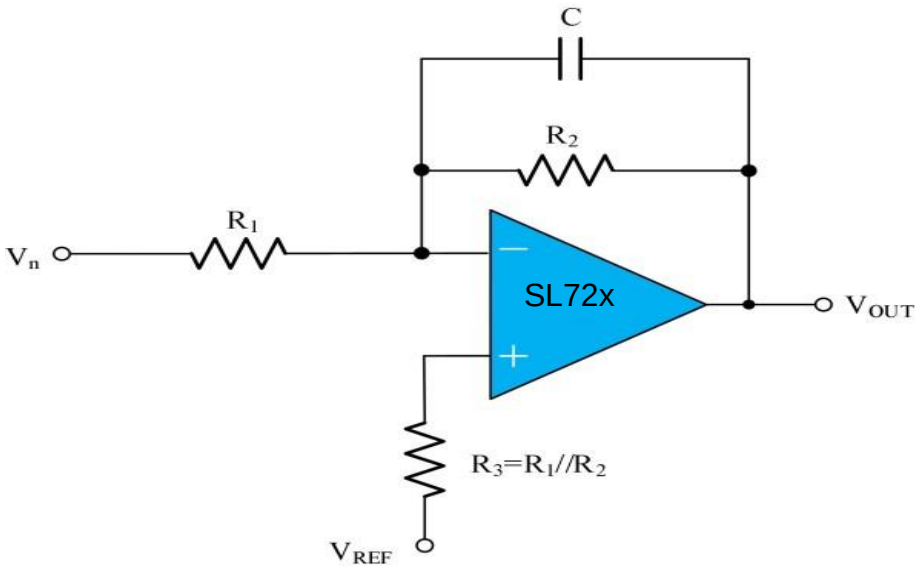
The circuit in Figure 17, like Figure 16, has high input impedance and performs the same function.



Instrumentation Amplifier

10. Active Low-Pass Filter

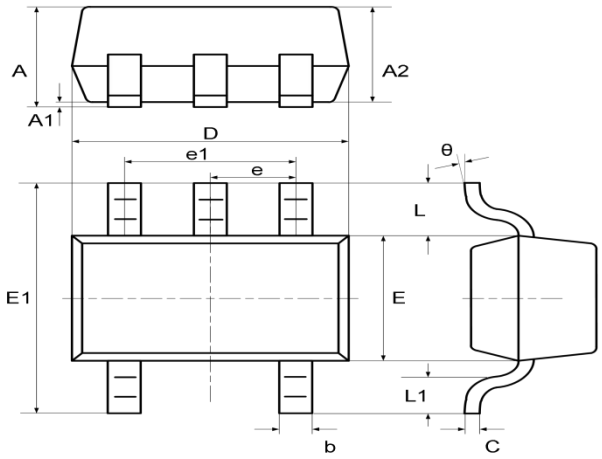
The DC gain of the low-pass filter shown in Figure 18 is (-R2/R1), and the -3dB cutoff frequency is 1/(2πR2C). Ensure that the filter bandwidth is within the amplifier's bandwidth. Large feedback resistors coupled with parasitic capacitance can cause adverse effects such as ringing or oscillation in high-speed amplifiers. Keep the resistor values as low as possible and consistent with considerations for the output load.



Active Low-Pass Filter

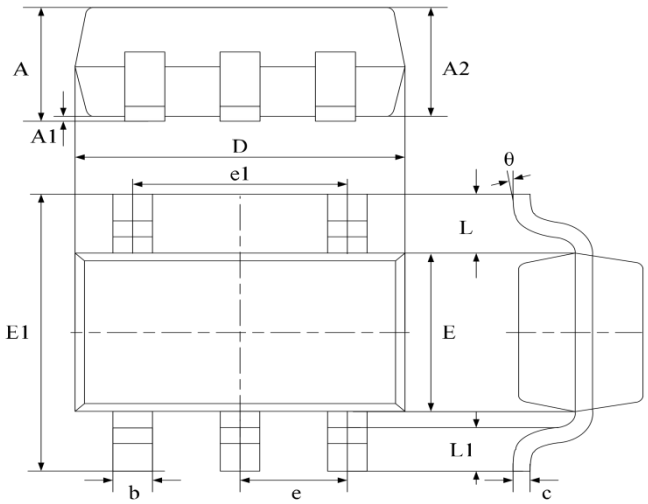
Package

SC70-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	0.900	0.035	0.039
b	0.150	0.350	0.006	0.014
C	0.080	0.150	0.003	0.006
D	1.8500	2.150	0.079	0.087
E	1.100	1.400	0.045	0.053
E1	1.950	2.200	0.085	0.096
e	0.850 Typ.		0.026 Typ.	
e1	1.200	1.400	0.047	0.055
L	0.42 ref.		0.021 ref.	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

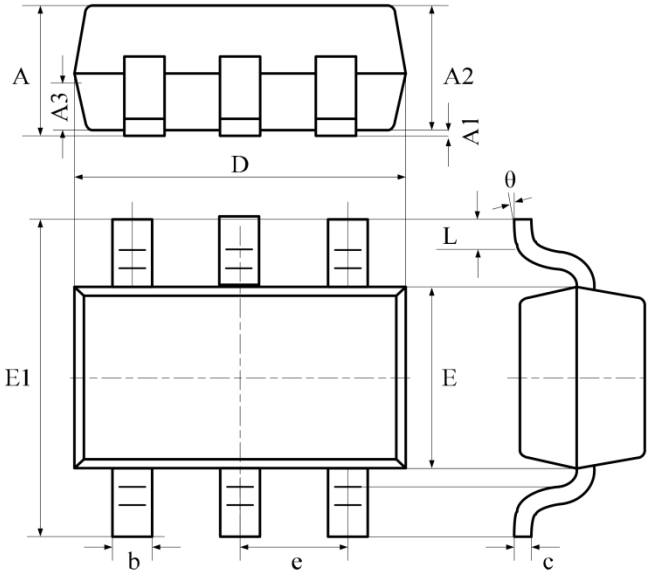
SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.040	1.350	0.042	0.055
A1	0.040	0.150	0.002	0.006
A2	1.000	1.200	0.041	0.049
b	0.380	0.480	0.015	0.020
c	0.110	0.210	0.004	0.009
D	2.720	3.120	0.111	0.127
E	1.400	1.800	0.057	0.073
E1	2.600	3.000	0.106	0.122
e	0.950 Typ.		0.037 Typ.	
e1	1.900 Typ.		0.078 Typ.	
L	0.700 ref.		0.028 ref.	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

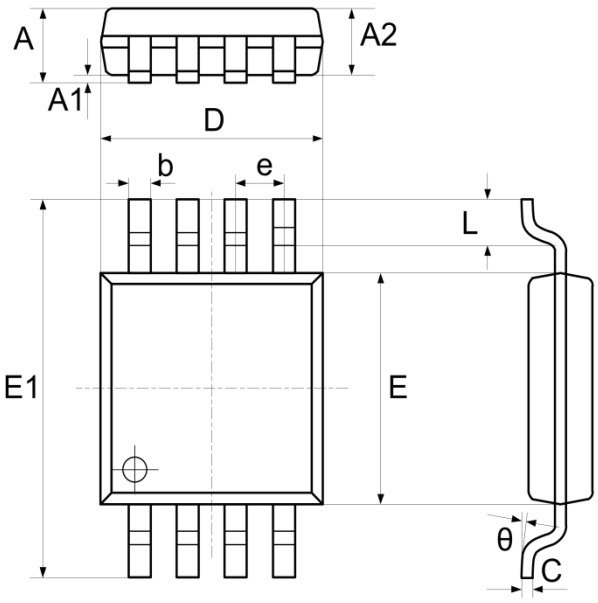
Package

SOT23-6



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	1.050	1.150	1.250
A1	0.000	0.060	0.150
A2	1.000	1.100	1.200
A3	0.550	0.650	0.750
D	2.820	2.920	3.020
E	1.510	1.610	1.710
E1	2.600	2.800	3.000
b	0.300	0.400	0.500
e	0.950BSC		
θ	0°	4°	8°
L	0.300	0.420	0.570
c	0.100	0.152	0.200

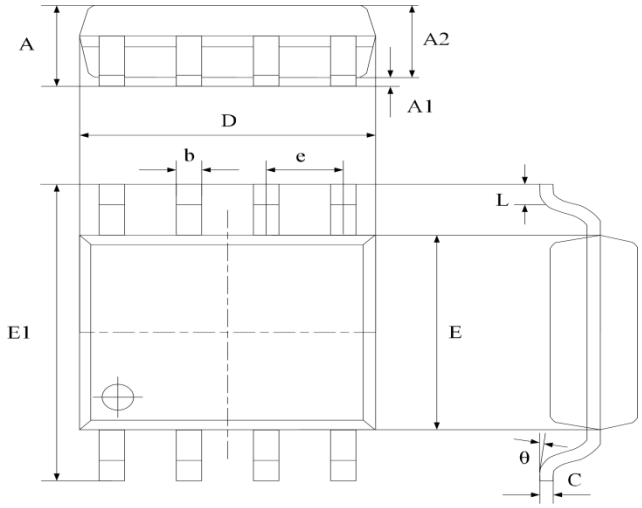
MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.033	0.045
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.031	0.039
b	0.290	0.380	0.012	0.016
C	0.150	0.200	0.006	0.008
D	2.900	3.100	0.118	0.127
E	2.900	3.100	0.118	0.127
E1	4.700	5.100	0.192	0.208
e	0.650 Typ.		0.026 Typ.	
L	0.400	0.700	0.016	0.029
θ	0°	8°	0°	8°

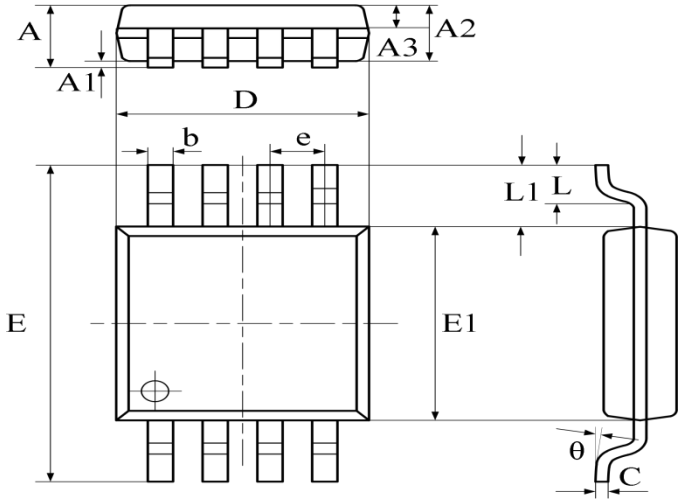
Package

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.370	1.670	0.056	0.068
A1	0.070	0.170	0.003	0.007
A2	1.300	1.500	0.053	0.061
b	0.306	0.506	0.013	0.021
C	0.203 Typ.		0.008 Typ.	
D	4.700	5.100	0.192	0.208
E	3.820	4.020	0.156	0.164
E1	5.800	6.200	0.237	0.253
e	1.270 Typ.		0.050 Typ.	
L	0.450	0.750	0.018	0.306
θ	0°	8°	0°	8°

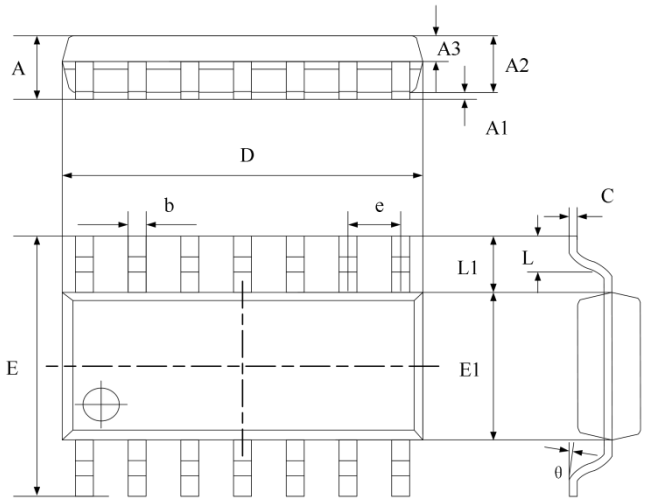
TSSOP-8



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.900	1.000	1.050
A3	0.390	0.440	0.490
b	0.200	-	0.280
C	0.130	-	0.170
D	2.900	3.000	3.100
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
e	0.65BSC		
L	0.450	-	0.750
L1	1.000 ref		
θ	0°	-	8°

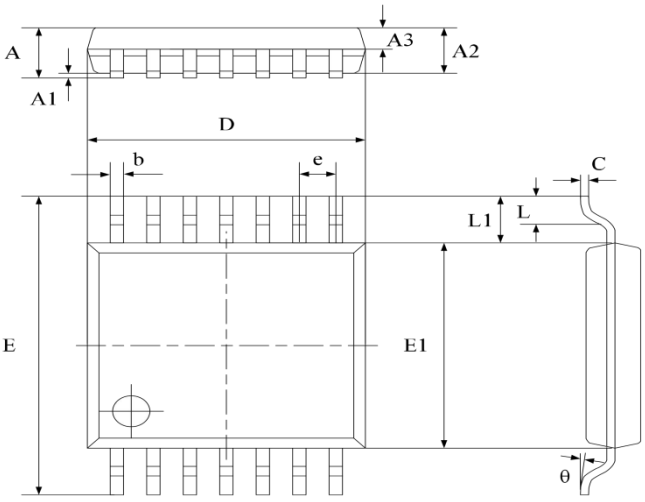
Package

SOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.450	1.850	0.059	0.076
A1	0.100	0.300	0.004	0.012
A2	1.350	1.550	0.055	0.063
A3	0.550	0.750	0.022	0.031
b	0.406typ.		0.017typ.	
C	0.203typ.		0.008typ.	
D	8.630	8.830	0.352	0.360
E	5.840	6.240	0.238	0.255
E1	3.850	4.050	0.157	0.165
e	1.270 Typ.		0.050 Typ.	
L1	1.040 ref.		0.041 ref.	
L	0.350	0.750	0.014	0.031
θ	2°	8°	2°	8°

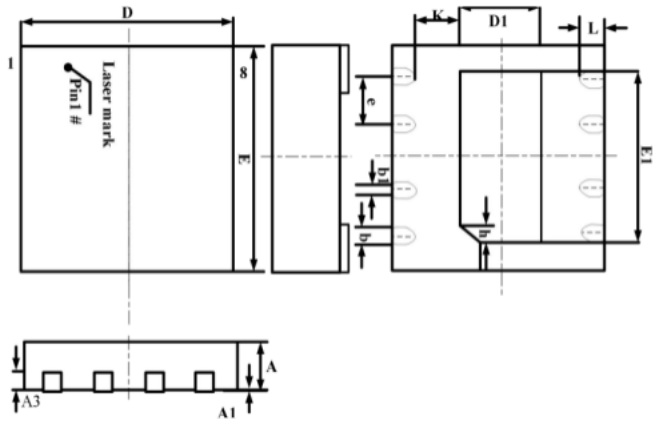
TSSOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.200	-	0.0472
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.037	0.043
A3	0.390	0.490	0.016	0.020
b	0.200	0.290	0.008	0.012
C	0.130	0.180	0.005	0.007
D	4.860	5.060	0.198	0.207
E	6.200	6.600	0.253	0.269
E1	4.300	4.500	0.176	0.184
e	0.650 typ.		0.0256 typ.	
L1	1.000 ref.		0.0393 ref.	
L	0.450	0.750	0.018	0.031
θ	0°	8°	0°	8°

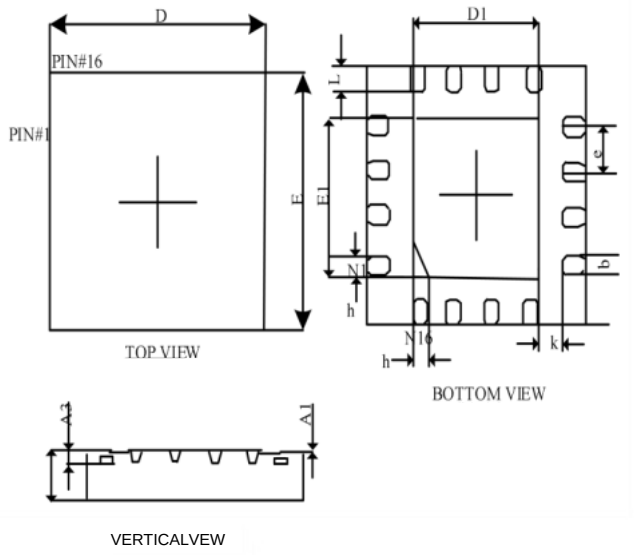
Package

DFN8-L2*2



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	0.203REF		
b	0.200	0.2500	0.300
b1	0.180REF		
D	1.900	2.000	2.100
E	1.900	2.000	2.100
e	0.500BSC		
D1	0.500	0.600	0.700
E1	1.100	1.200	1.300
L	0.300	0.350	0.40
K	0.35REF		
h	0.200REF		

QFN16-L3*3



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	0.203REF		
b	0.200	0.2500	0.300
D	2.900	3.000	3.100
E	2.900	3.000	3.100
e	0.500BSC		
D1	1.700	1.800	1.900
E1	1.700	1.800	1.900
L	0.200	0.300	0.400
K	0.300REF		
h	0.300REF		