480 µA, 6.5MHz, RRIO CMOS Operational Amplifier

Description

- SL8631 (single-channel), SL8632 (dual-channel), and SL8634 (quad-channel) are operational amplifiers designed for low noise, low voltage, and low power applications.The SL863x series features a bandwidth of 6.5MHz, a slew rate of 4V/µs, and a static current of 480µA per amplifier (at a 5V supply voltage). They are suitable for various applications.

- The SL863x operational amplifiers are widely used in low-voltage and low-noise systems to provide optimal performance. Their input common-mode voltage range includes ground, with a maximum input offset voltage of 4.2mV.SL863x amplifiers can drive rail-to-rail output swings under heavy output loads.

- The SL863x series operates with single supplies from +2.1V to +5.5V or dual supplies. All models are specified to operate within an extended industrial temperature range of -40°C to +125°C.

- SL8631 is available in 5-pin SC70 and SOT-23 packages. SL8632 is offered in 8-pin MSOP, DFN2*2, TSSOP, and SOP packages. SL8634 is packaged in 14-pin TSSOP and SOP configurations.

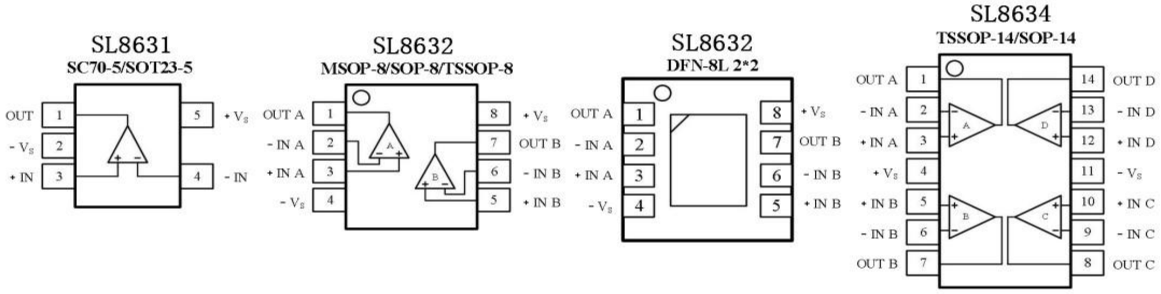
Feature

- High Slew Rate: 4V/µs
- Gain-Bandwidth Product: 6.5MHz
- Low Power Consumption: 480µA per amplifier
- 0.1% Settling Time (for a 2V step): 1µs
- Low Noise: 20nV/√Hz@10kHz
- High Gain: 103dB
- Low Offset Voltage: 4.2mV (maximum)
- Unity Gain Stable
- Rail-to-Rail Input and Output ----- Input Voltage Range: -0.1V to +5.1V (at 5V supply voltage)
- Operating Supply Range: +2.1V to +5.5V
- Operating Temperature Range: -40°C to +125°C

Application

- Photodiode and sensor interfaces
- Audio output
- Active filters
- Driving A/D converters
- Portable devices and battery-powered equipment

Pin configuration



Pin Arrangement

Pin function

Pin Name	Description
-IN	negative (inverting) input terminal.
+IN	positive (non-inverting) input terminal.
-INA, -INB -INC, -IND	the voltage range for the amplifier's inverting input can go from (V_{S-} – 0.1V) to (V_{S+} + 0.1V).
+INA,+INB +INC, +IND	the amplifier's non-inverting input terminal has the same voltage range as –IN.
$+V_S$	positive supply terminal, voltage ranges from 2.1V to 5.5V. A 0.1μF bypass capacitor should be placed as close as possible to the device, either between power pins or between power pins and ground.
$-V_S$	negative supply terminal, typically connected to ground. It can also be connected to a voltage outside ground as long as the voltage between V_{S+} and V_{S-} is within 2.1V to 5.5V. If not grounded, a 0.1μF capacitor should be placed as close as possible to ground near the device.
OUTA, OUTB OUTC, OUTD	amplifier output terminal.
OUT	output terminal.

Ordering information

PN	Package	Quantity
SL8631XC5	SC70-5	PEC, 3000
SL8631XT5	SOT23-5	PEC, 3000
SL8632XS8	SOP-8	PEC, 4000
SL8632XV8	MSOP-8	PEC, 3000
SL8632XF8	DFN-8	PEC, 3000
SL8632XT8	TSSOP-8	PEC, 3000
SL8634XT14	TSSOP-14	PEC, 3000
SL8634XS14	SOP-14	PEC, 2500

Absolute maximum rating (T$_A$=25℃)

Symbol	Parameter	Value	Unit
V_{S+}, V_{S-}	supply voltage， V_{S+} to V_{S-}	7.0	V
V_{CM}	common-mode input voltage	V_{S-} –0.3 to V_{S+} +0.3	V
ESD	electrostatic discharge voltage	HBM ±4000	V
		CDM ±1000	V
T_J	junction temperature	160	°C
T_{STG}	storage temperature range	-65 to +150	°C
T_{JL}	soldering temperature range (10 seconds soldering)	260	°C

Note:

1. Exceeding the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Prolonged exposure to absolute maximum ratings conditions may affect device reliability.

2. Input terminals are clamped to the power supply rails with diodes.

3. The provided device will never exceed the maximum junction temperature (T_J) at any time.

Electrical Parameter

（V_S = 5V, T_A = +25℃, V_{CM} = V_S/2, V_O = V_S/2, R_L = 10kΩ connect to V_S/2, Unless otherwise specified）

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
input characteristics						
V_{OS}	input offset voltage		-4.2	±0.8	+4.2	mV
	full temperature range		-4.5		+4.5	
$V_{OS}TC$	offset voltage drift			2		μV/°C
I_B	input bias current			1		pA
	full temperature			800		
I_{OS}	input offset current			1		pA
V_{CM}	common-mode voltage range		V_{S-}–0.1		V_{S+}+0.1	V
CMRR	common-mode rejection ratio	V_{CM} = 0.05V to 3.5V	66	84		dB
	full temperature			80		
		V_{CM} = V_{S-}–0.1V to V_{S+}+0.1V	60	76		
A_{VOL}	open-loop voltage gain	R_L = 10kΩ, V_O = 0.05 to 3.5V	90	103		
	full temperature			90		
		R_L = 600Ω, V_O = 0.15 to 3.5V	77	86		
	full temperature			80		
R_{IN}	input resistance			100		GΩ
C_{IN}	input capacitance	differential mode		2.0		pF
		common mode		3.5		
output characteristics						
V_{OH}	high output voltage swing	R_L = 600Ω		V_{S+}–130		mV
		R_L = 10kΩ		V_{S+}–12		
V_{OL}	low output voltage swing	R_L = 600Ω		120		mV
		R_L = 10kΩ		7		
Z_{OUT}	closed-loop output impedance	f = 200kHz, G = +1		0.4		Ω
	open-loop output impedance	f = 1MHz, I_O = 0		2.6		
I_{SC}	short-circuit current	pull-up current		40		mA
		pull-down current		40		

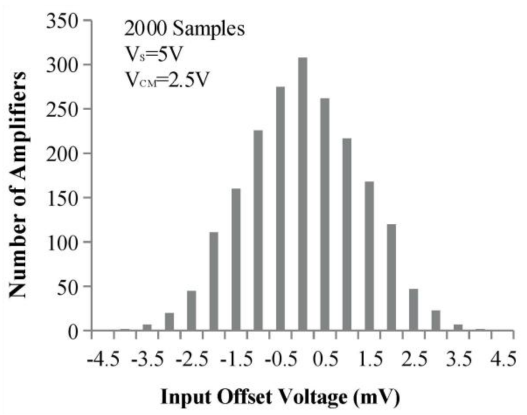
Electrical Parameter

（V_S = 5V, T_A = +25℃, V_{CM} = V_S/2, V_O = V_S/2, R_L = 10kΩ connect to V_S/2, Unless otherwise specified）

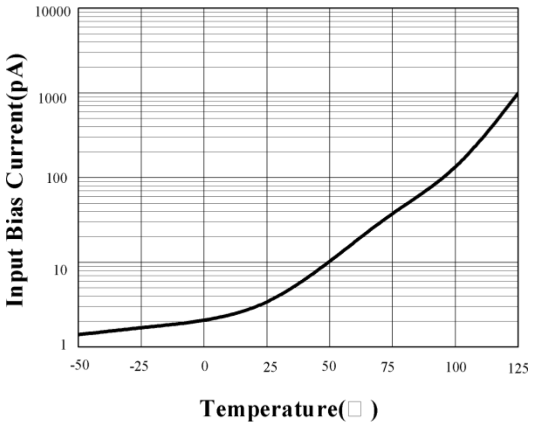
Parameter	Symbol	Condition	Min	Typ	Max	Unit
power supply characteristics						
GBW	gain bandwidth product			6.5		MHz
$Φ_M$	phase margin	C_L = 100pF		60		°
SR	slew rate	G = +1, C_L = 100pF, V_O = 1.5V to 3.5V		4		V/μs
BW_P	full power bandwidth	<1% Distortion		300		kHz
t_S	settling time overload recovery time	0.1%, G = +1（2V Step）		1		μs
		0.01%, G = +1（2V Step）		1.2		
t_{OR}	full power bandwidth	V_{IN} × Gain > V_S		0.5		μs
noise characteristics						
V_n	input voltage noise	f = 0.1 to 10 Hz		12		μVP-P
e_n	input voltage noise density	f = 10kHz		20		nV/√Hz
I_n	input current noise density	f = 10kHz		5		fA/√Hz
power supply						
V_S	power supply voltage		2.1		5.5	V
PSRR	power supply rejection ratio	V_S = 2.7V to 5.5V, V_{CM} < V_{S+} − 2V	70	84		dB
	full temperature			80		
I_Q	quiescent current (per amplifier)			480	560	μA
	full temperature			520	620	
thermal characteristics						
T_A	temperature range		-40		+125	°C
$θ_{JA}$	package thermal impedance	SC70-5		333		°C/W
		SOT23-5		190		
		MSOP-8		216		
		SO-8		125		
		DFN-8L		201		
		TSSOP-8		153		
		TSSOP-14		112		
		SO-14		115		

Typical characteristics curves

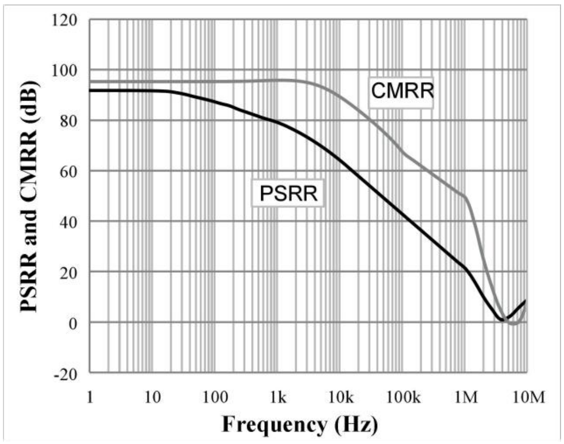
（T_A=+25℃, V_{CM}=V_S/2, RL=10kΩ connect to V_S/2, Unless otherwise specified）



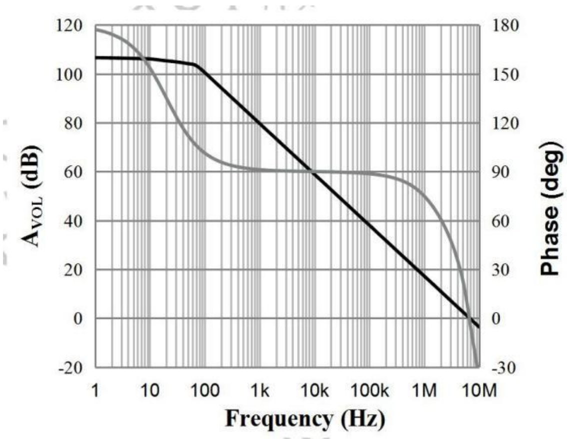
Input offset voltage distribution



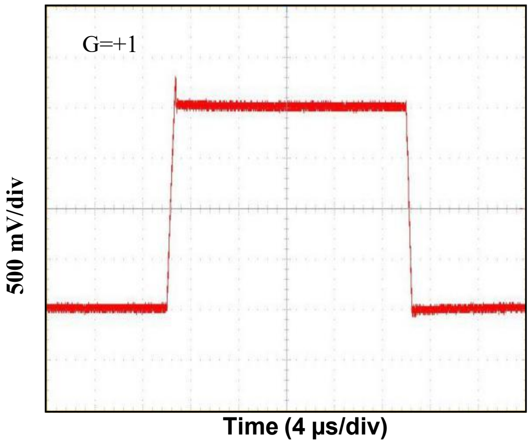
Relationship between input bias current and temperature



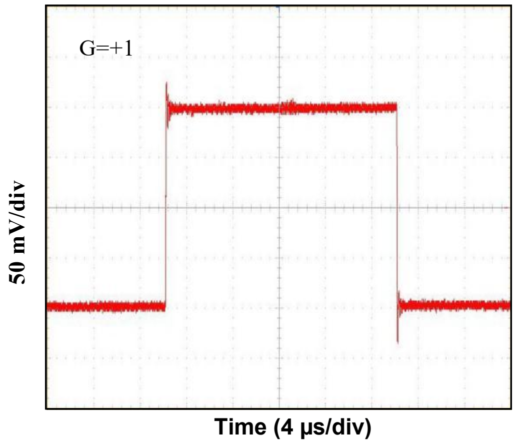
Power supply rejection ratio and
common mode rejection ratio versus frequency



Open-loop gain and phase margin versus frequency



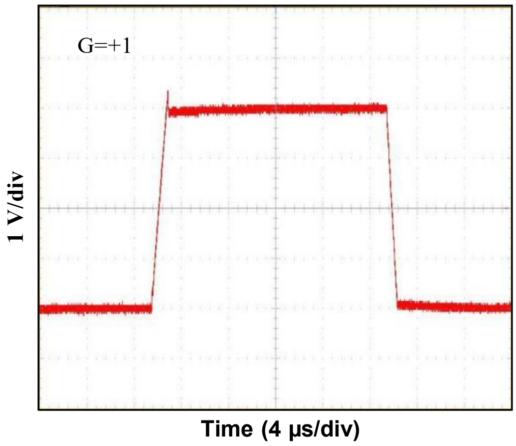
Large signal step response at 2.7V



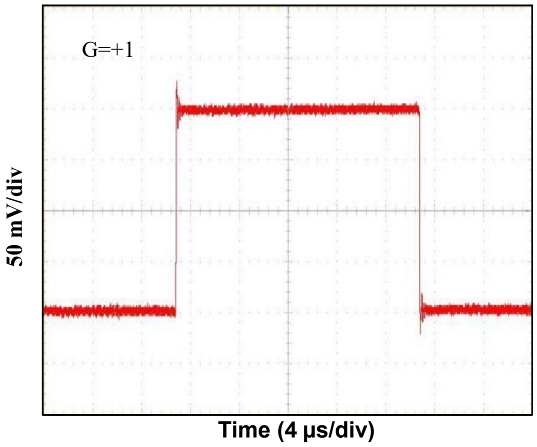
Small signal step response at 2.7V

Typical characteristics curves

（T_A = +25℃, V_{CM} = V_S/2, R_L = 10kΩ connect to V_S/2, Unless otherwise specified）



Large signal step response at 5V



Small signal step response at 5V

Application

1. Low input bias current

The SL863x is a series of CMOS operational amplifiers known for their extremely low input bias currents in the pA range. The low input bias current allows the amplifier to be used in applications with high-resistance sources, but care must be taken to minimize PCB surface leakage currents. For more details, please refer to the "PCB Surface Leakage" section below.

2. PCB Surface Leakage

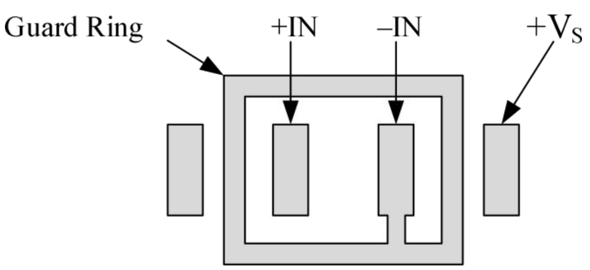
In applications that demand low input bias currents, consideration must be given to the phenomenon of surface leakage on printed circuit boards (PCB). Surface leakage is caused by moisture, dust, or other contaminants present on the PCB. Under low humidity conditions, the typical resistance between adjacent traces can be as high as 10^12 ohms. A voltage difference of 5V between them can result in a current flow of 5pA, which exceeds the input bias current of the SL863x operational amplifier at +25℃ (typical value ±1pA).

It is recommended to employ a multilayer PCB layout and route the –IN and +IN signals of the operational amplifier beneath the PCB surface to mitigate surface leakage effects.

An effective method to reduce surface leakage is to use guard rings around sensitive pins (or traces). These guard rings are biased at the same voltage as the sensitive pins. Such a layout example for an inverting gain application is illustrated in Figure 10.

1. For non-inverting gain and unity gain buffers:
   a) Use wires that do not contact the PCB surface to connect the non-inverting input pin (+IN) to the input.
   b) Connect a guard ring to the inverting input pin (-IN). This biases the guard ring to the common-mode input voltage.

2. For inverting gain and transimpedance amplifiers (converting current to voltage, e.g., for photodetectors):
   a) Connect a guard ring to the non-inverting input pin (+IN). This biases the guard ring to the same reference voltage as the operational amplifier (e.g., VS/2 or ground).
   b) Use wires that do not contact the PCB surface to connect the inverting input pin (-IN) to the input.

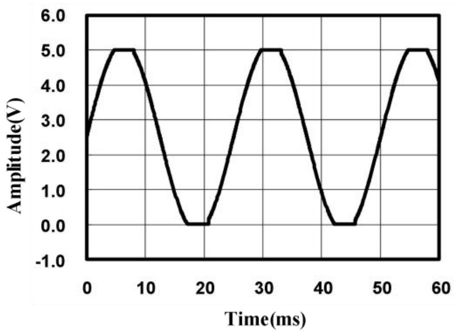


Using guard rings around sensitive pins.

3. Rail-to-Rail Feature

The SL863x series has an input common-mode voltage range that can exceed the power supply rails by 300mV. This is achieved through a complementary input stage — a parallel combination of an N-type MOS input differential pair and a P-type MOS input differential pair. For normal operation, inputs should be limited within this range. The absolute maximum input voltage exceeds the power supply voltage by 500mV.

Inputs that are outside the input common-mode range but below the maximum input voltage are ineffective but do not cause any damage to the op-amp.Unlike some other operational amplifiers, if the input current is limited, the input may exceed the power supply without phase inversion, as shown in Figure 11. Due to the extended input common-mode range from (VS- - 0.1V) to (VS+ + 0.1V), the SL863x operational amplifier can achieve 'true ground' detection.



Phase free flipping when the input exceeds the power supply voltage

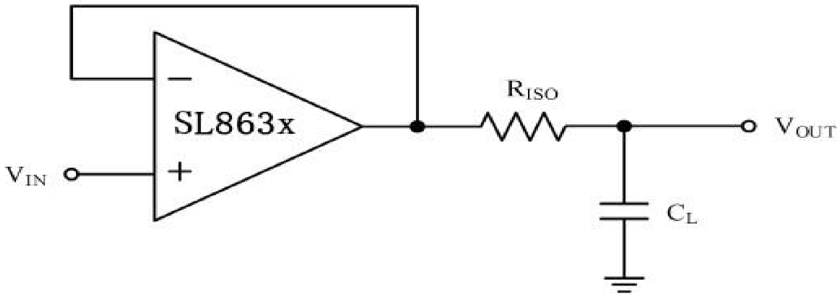
The AB class output stage topology of the common-source transistor can achieve rail-to-rail output. For light resistive loads (e.g., 100kΩ), the output voltage typically swings to within 5mV of the power supply rails. Under moderate resistive loads (e.g., 10kΩ), the output can swing to within 15mV of the power rails while maintaining high open-loop gain.The maximum output current depends on the total power supply voltage. As the amplifier's power supply voltage increases, so does its output current capability. When the output is continuously short-circuited, care must be taken to keep the IC junction temperature below 150°C.

The amplifier's output includes reverse-biased ESD diodes connected to each power supply. The output should not be forced beyond 0.5V of either power supply, as this would cause current to flow through these diodes.

4. Capacitive Load and Stability

The SL863x can directly drive 1nF at unity gain without oscillation. Unity gain followers (buffers) are the circuits most sensitive to capacitive loads.

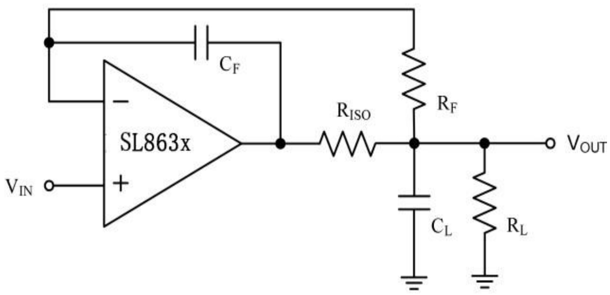
Directly driving capacitive loads can reduce the phase margin of the amplifier, leading to ringing or even oscillation. Applications requiring higher capacitive drive capability should use isolation resistors between the output and the capacitive load, as shown in Figure 12. The isolation resistor R_{ISO} and the load capacitor C_L form a zero to improve stability. A larger value of R_{ISO} provides more stable V_{OUT}. Note that this method causes gain accuracy loss because R_{ISO} forms a voltage divider with R_L.



Indirectly drive capacitive load

Improve the circuit as shown in Figure 13. It ensures DC precision while also maintaining AC stability. R_F provides DC precision by connecting the inverted signal to the output.

C_F and R_{ISO} maintain phase margin throughout the feedback loop by feeding back high-frequency components of the output signal to the amplifier's inverting input, compensating for phase margin loss.



Driving capacitive loads with DC precision indirectly.

For circuits with non-unity gain, there are two additional methods to increase phase margin: (a) by increasing the amplifier gain, or (b) by paralleling capacitors with feedback resistors to cancel parasitic capacitance associated with the inverting node.

5. Power Supply Layout and Filtering

The SL863x series operates with a single supply from +2.1V to +5.5V or dual supplies from ±1.05V to ±2.25V. For single-supply operation, filtering ceramic capacitors (0.01μF to 0.1μF) should be placed within 2mm of the VS pin to achieve good high-frequency performance.

In dual-supply operation, separate 0.1μF ceramic capacitors should be connected to ground for both VS+ and VS– power supplies. Larger capacitors (2.2μF or greater tantalum capacitors)within 100mm can provide large and slow current and improve overall performance. These larger capacitors can be shared with other analog devices.

Effective PCB layout techniques optimize performance by reducing stray capacitance at the inputs and outputs of operational amplifiers. To minimize stray capacitance, external components should be placed as close to the chip as possible, minimizing trace lengths and widths, and utilizing surface-mount devices wherever feasible.

For operational amplifiers, it is strongly recommended to solder devices directly onto the PCB to minimize loop area for high-frequency and high-current paths, thus reducing EMI (electromagnetic interference).

6. Grounding

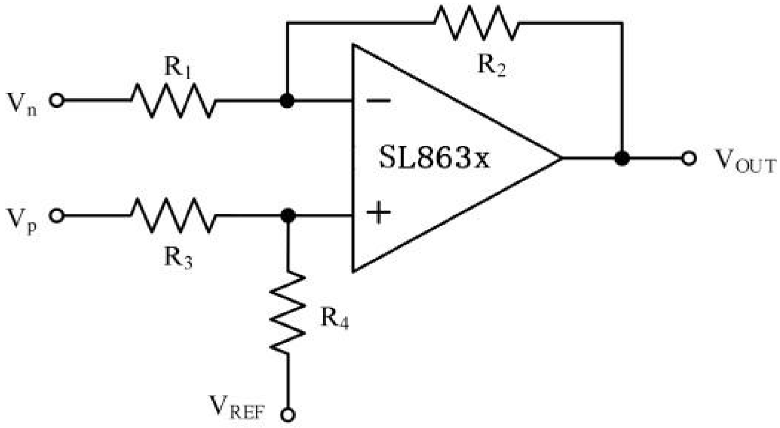
In SL863x circuit design, the ground plane is critical. The length of current paths in the ground return lines can generate unwanted voltage noise, and a wide ground area helps to reduce parasitic inductance.

7. Input-Output Coupling

To minimize capacitive coupling, input and output signal traces should not be routed parallel to each other. This helps reduce undesired positive feedback.

Typical application circuit diagram

1. Differential Amplifier

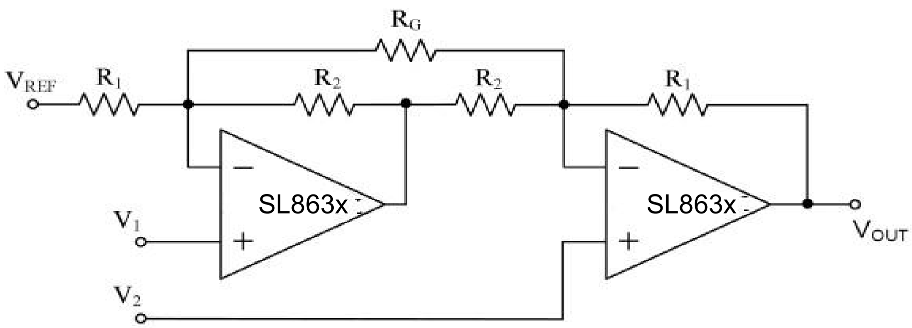


Figure

Circuit shown in Figure 14 implements differential functionality. If the resistance ratio is R4/R3 = R2/R1, then:

$$\mathbf{V_{OUT} = (V_p - V_n) \times R_2/R_1 + V_{REF}}$$

2. Instrumentation Amplifier



$$V_{OUT} = (V_1 - V_2)(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G}) + V_{REF}$$

Figure

The SL863x series is well-suited for conveying sensor signals in battery-powered applications. Figure 15 illustrates an instrumentation amplifier using two operational amplifiers from the SL863x series. This circuit is suitable for applications requiring high gain to suppress common-mode noise. The reference voltage (V_{REF}) is provided by a low impedance source. In single-supply voltage applications, V_{REF} is typically set to $V_S/2$.

Typical application circuit diagram

3. Chemical Sensor

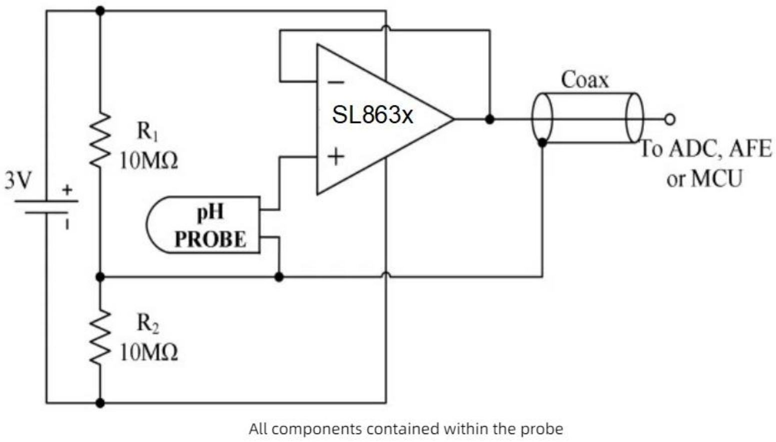


Figure pH probe

The input bias current of the SL863x series is within the pA range, making it an ideal choice for buffering high-impedance chemical sensors such as pH probes. For instance, the circuit in Figure 16 eliminates the need for expensive low-leakage cables when connecting pH probes (like the universal combination pH probe, e.g., Corning 476540) to measurement ICs such as ADCs, AFEs, and/or MCUs.

An SL863x operational amplifier and a lithium battery are integrated into the probe assembly. Traditional low-cost coaxial cables are used to transmit the output signal of the operational amplifier to subsequent ICs for pH value reading.

4.Current Sensing Amplifier Based on Shunt

The slew rate of the current sensing amplifier output sinusoidal signal shown in Figure 17 is $2\pi f_{VPP}$, and the slew rate of the output triangular wave signal is 2fVPP. In most motor control systems, PWM frequencies range from 10kHz to 20kHz. For a PWM frequency of 10kHz, one period lasts 100μs. In motor current sensing, phase currents are converted to phase voltage signals for ADC sampling.

This sampling voltage signal must be established before entering the ADC. As shown in Figure 8, the total establishment time of the current shunt monitor circuit includes: the rise delay time (t_{SR}) due to the slew rate of the operational amplifier, and the measurement establishment time (t_{SET}).

If the minimum duty cycle of PWM is defined as 5%, and t_{SR} needs to perform phase current monitoring at 20% of the total time window, for a 3.3V motor control system (with a 12-bit ADC of 3.3V MCU), the slew rate of the operational amplifier should be greater than:

$$3.3V/(100\mu s\times5\%\times20\%)=3.3V/\mu s$$

Simultaneously, the bandwidth of the operational amplifier should be significantly greater than the PWM frequency (at least 10 times higher).

Typical application circuit diagram

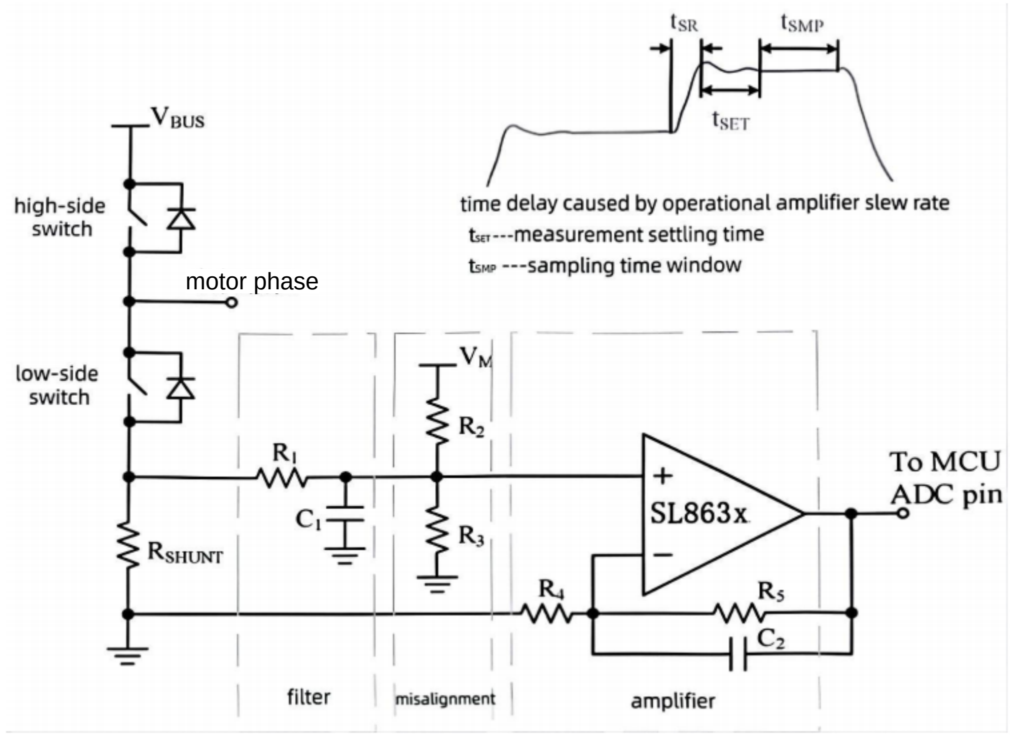
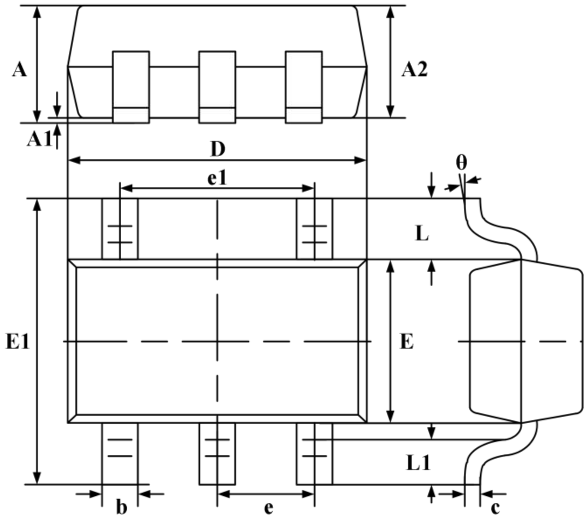


Figure current shunt monitoring circuit

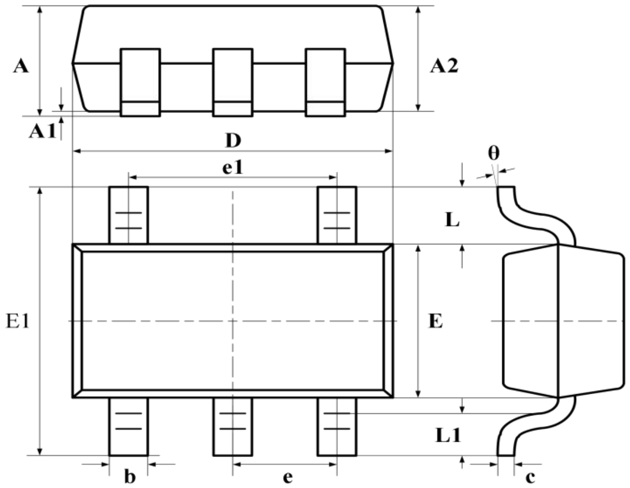
Package

SC70-5 (SOT353)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	0.900	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D	1.850	2.150	0.079	0.087
E	1.100	1.400	0.045	0.053
E1	1.950	2.200	0.085	0.096
e	0.850 typ.		0.026 typ.	
e1	1.200	1.400	0.047	0.055
L	0.42 ref.		0.021 ref.	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

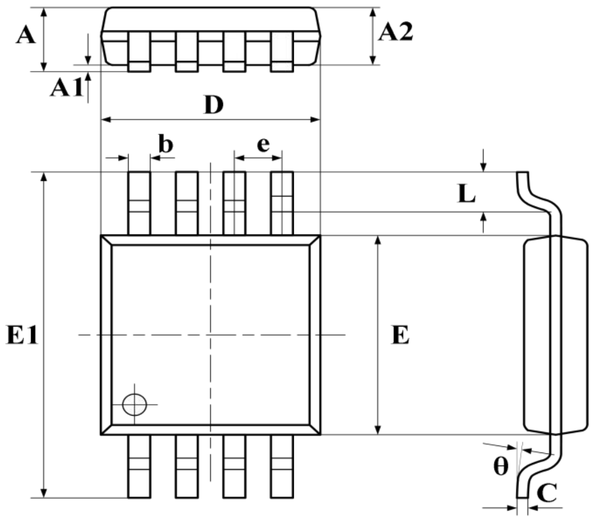
SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.040	1.350	0.042	0.055
A1	0.040	0.150	0.002	0.006
A2	1.000	1.200	0.041	0.049
b	0.380	0.480	0.015	0.020
c	0.110	0.210	0.004	0.009
D	2.720	3.120	0.111	0.127
E	1.400	1.800	0.057	0.073
E1	2.600	3.000	0.106	0.122
e	0.950 typ.		0.037 typ.	
e1	1.900 typ.		0.078 typ.	
L	0.700 ref.		0.028 ref.	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

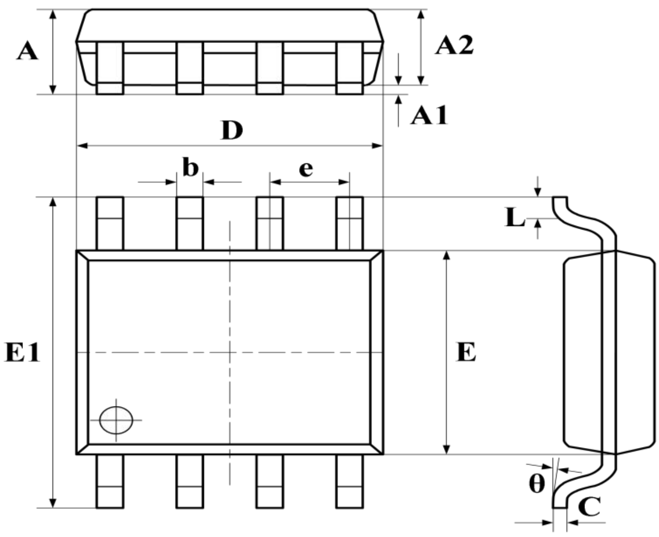
Package

MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.033	0.045
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.031	0.039
b	0.290	0.380	0.012	0.016
C	0.150	0.200	0.006	0.008
D	2.900	3.100	0.118	0.127
E	2.900	3.100	0.118	0.127
E1	4.700	5.100	0.192	0.208
e	0.650 typ.		0.026 typ.	
L	0.400	0.700	0.016	0.029
θ	0°	8°	0°	8°

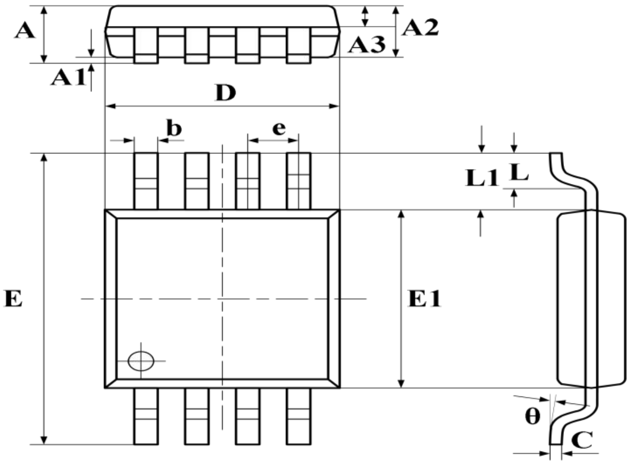
SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.370	1.670	0.056	0.068
A1	0.070	0.170	0.003	0.007
A2	1.300	1.500	0.053	0.061
b	0.306	0.506	0.013	0.021
C	0.203 typ.		0.008 typ.	
D	4.700	5.100	0.192	0.208
E	3.820	4.020	0.156	0.164
E1	5.800	6.200	0.237	0.253
e	1.270 typ.		0.050 typ.	
L	0.450	0.750	0.018	0.306
θ	0°	8°	0°	8°

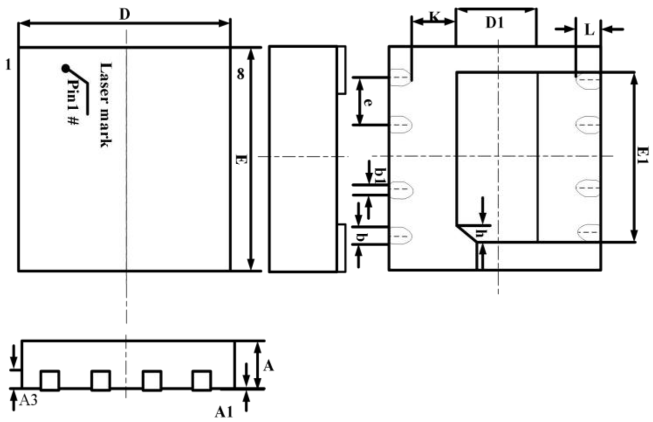
Package

TSSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches
	Min	Typ	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.900	1.000	1.050
A3	0.390	0.440	0.490
b	0.200	-	0.280
C	0.130	-	0.170
D	2.900	3.000	3.100
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
e	0.65BSC		
L	0.450	-	0.750
L1	1.000 ref		
θ	0°	-	8°

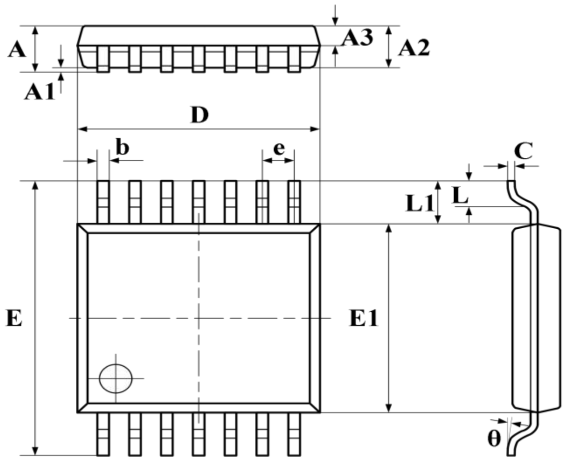
DFN8-L 2*2



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	0.203REF		
b	0.200	0.2500	0.300
b1	0.180REF		
D	1.900	2.000	2.100
E	1.900	2.000	2.100
e	0.500BSC		
D1	0.500	0.600	0.700
E1	1.100	1.200	1.300
L	0.300	0.350	0.40
K	0.35REF		
h	0.200REF		

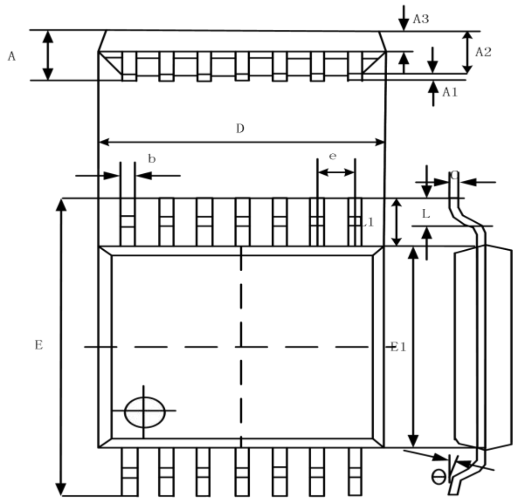
Package

TSSOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.200	-	0.0472
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.037	0.043
A3	0.390	0.490	0.016	0.020
b	0.200	0.290	0.008	0.012
C	0.130	0.180	0.005	0.007
D	4.860	5.060	0.198	0.207
E	6.200	6.600	0.253	0.269
E1	4.300	4.500	0.176	0.184
e	0.650 typ.		0.0256 typ.	
L1	1.000 ref.		0.0393 ref.	
L	0.450	0.750	0.018	0.031
θ	0°	8°	0°	8°

SOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.450	1.850	0.059	0.076
A1	0.100	0.300	0.004	0.012
A2	1.350	1.550	0.055	0.063
A3	0.550	0.750	0.022	0.031
b	0.406typ.		0.017typ.	
C	0.203typ.		0.008typ.	
D	8.630	8.830	0.352	0.360
E	5.840	6.240	0.238	0.255
E1	3.850	4.050	0.157	0.165
e	1.270 typ.		0.050 typ.	
L1	1.040 ref.		0.041 ref.	
L	0.350	0.750	0.014	0.031
θ	2°	8°	2°	8°