Monolithic low dropout fixed voltage regulator

1. Description

The SL4275-G is a 5-pin TO packaged single-chip integrated low dropout voltage regulator. It regulates input voltages as high as 42V down to a 5.0V output voltage, VQ. This chip can drive loads up to 450mA and includes short-circuit and over-temperature protection features. When the typical output voltage VQ drops below 4.65V, the RQ pin of the chip generates a low-level reset signal, with the reset delay time adjustable via the capacitor connected to the D pin.

1.1 、External component information

The SL4275-G requires input capacitor CI to compensate for trace effects. To ensure stability of the regulation circuit, an output capacitor CQ is essential. Within the operating temperature range, an output capacitor with a capacitance (CQ) of at least 22uF and an equivalent series resistance (ESR) of no more than 5Ω will guarantee stability.

1.2 、Circuit description

The operational amplifier controls a reference voltage compared with a voltage proportional to the output voltage, driving the gate of a series MOSFET through a buffer. Additionally, a current limit control unit for the load prevents power components from entering saturation. The chip also integrates various internal circuits for protection against overload, overtemperature, and other conditions.

1.3 、Features

- Rated output voltage: 5V, with ±2% accuracy
- Ultra-low power consumption: 80uA
- Power-on and undervoltage reset
- Low dropout
- Short-circuit protection
- RoHS compliant

2. Principle block diagram

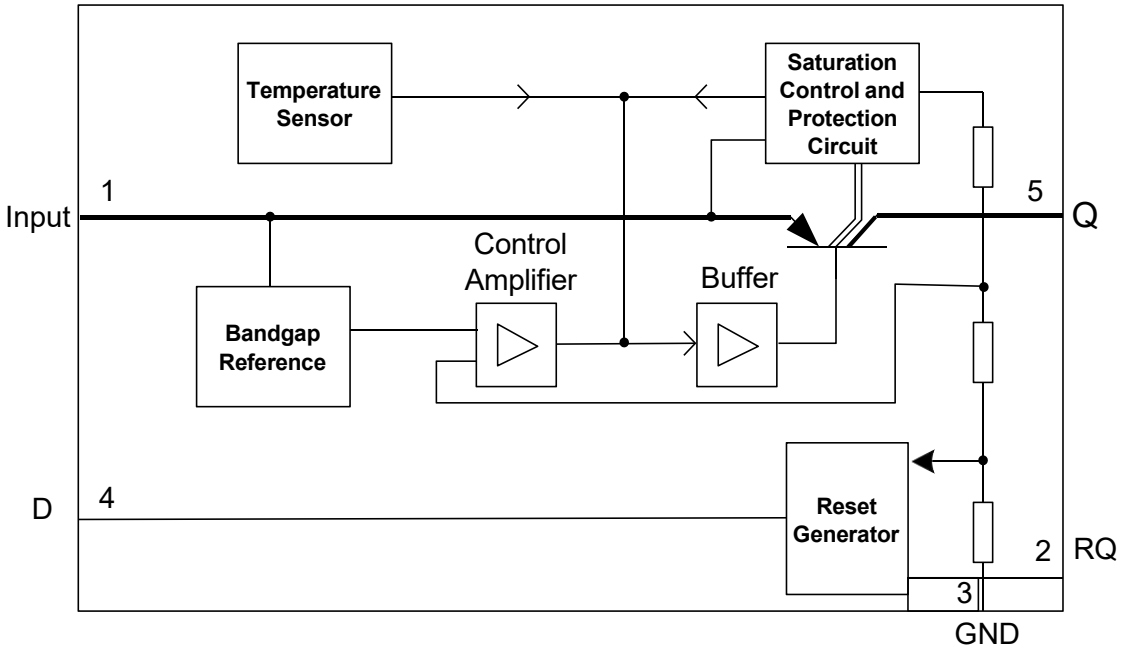


Fig.2-1 Module Block Diagram

3. Pin definition

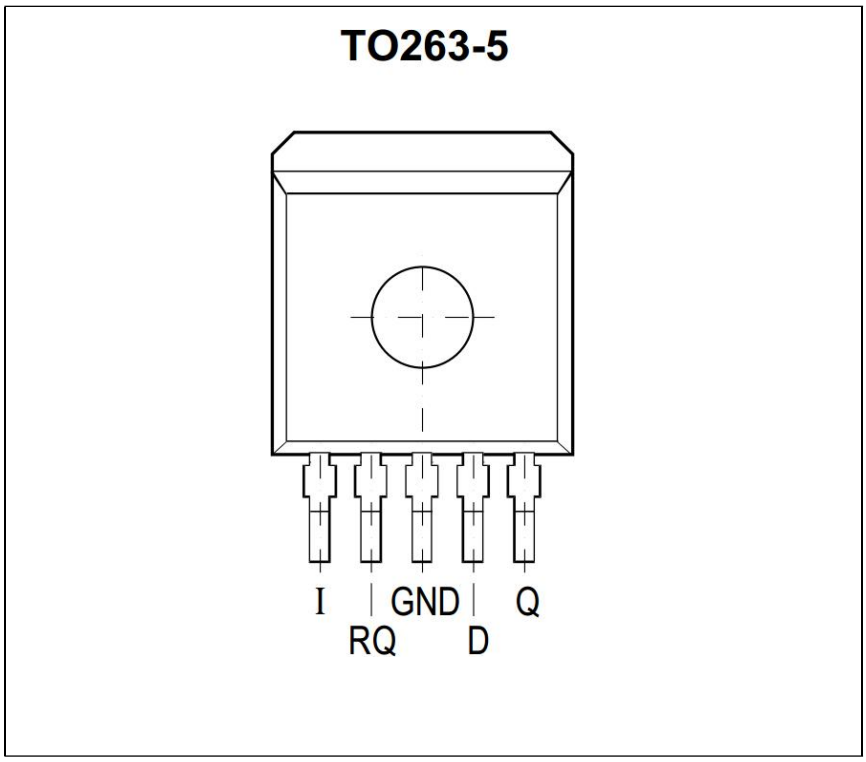


Fig.3-1 Pin Configuration (Top View)

Table 3.1 Pin Definition And Function

Pin Number	Symbol	Function
1	I	Input: Connect directly to ground with a ceramic capacitor close to the IC.
2	RQ	Reset output: The drain-source open circuit output pin requires an external pull-up resistor. When the output voltage drops below the reset threshold VRT, RQ is pulled low; it can be left floating when not in use.
3	GND	Ground: Internally connected to the heat sink.
4	D	Reset delay: Connect a capacitor to ground to set the reset delay time; it can be left floating when not in use.
5	Q	Output: Connect a capacitor to ground with CQ ≥ 22uF and ESR < 5Ω when operating at 10kHz.

4. General product characteristics

Table 4.1 Maximum Ratings

T_j = -40°C to 150°C. Unless otherwise specified, all voltages are relative to ground.

Paramerer	Symbol	Limit Value		Unit	Remark
		Min.	Max.		
input voltage	V_I	-0.3	42	V	
output voltage	V_Q	-0.3	12	V	
temperature	T_j	-40	150	℃	junction temperature
	T_{stg}	-40	150	℃	storage temperature
thermal resistance	R_{thj-a}	50	90	K/W	pin only
ESD withstand voltage	$V_{ESD-HBM}$	-2000	2000	V	human body model (1)
	$V_{ESD-CDM}$	-1000	1000	V	charged device model (2)

1) ESD withstand voltage per Human Body Model according to JESD22-A114.

2) ESD withstand voltage per Charged Device Model according to JESD22-C101E.

Table 4.2 Thermal Resistance

Parameter	Symbol	Limit Value			Unit	Conditions
		Min.	Typ.	Max.		
thermal resistance to case	RthJC		3.6		K/W	measuring the heat sink
junction to ambient thermal resistance	RthJA		22		K/W	
			74		K/W	pins only
			42		K/W	300 mm_2 heat sink
			34		K/W	600 mm_2 heat sink

1) It does not refer to production testing, but specifically to design;

5. Electrical characteristics

Table 5.1 Electrical characteristics

V_I = 13.5V; -40℃ ≤ T_j ≤ 150℃, Unless otherwise stated.

Parameter	Symbol	Parameter Value			Unit	Conditions
		Min.	Typ.	Max.		
operating voltage	V_I	5.5	13.5	42	V	
output voltage	V_Q	4.9	5.0	5.1	V	I_Q<450m;V_I<42V
output current limit	I_Q	450	800		mA	V_I=13.5V
quiescent current	I_{q1}		80	100	uA	I_Q = 5mA
static current	I_{q2}			0.5	mA	I_Q = 400mA
voltage drop	Vdr		0.3	0.5	V	I_Q = 300mA
load regulation	ΔVQLo			150	mV	5mA<I_Q<450mA
line regulation	ΔVQLi		2	10	mV	8V<V_I<40V,I_Q=5mA
power supply rejection ratio	PSRR		70		dB	100HZ@0.5Vpp
output capacitance	C_Q	1			uF	ESR≤5Ω@10KHZ
Reset output RQ:						
reset threshold	V_{RT}	4.5	4.65	4.8	V	output voltage drop
reset hysteresis	V_{hys}		0.2		V	
reset response time	t_{rr}			2	us	
reset output low voltage	V_{RQL}			0.4	V	R_{ext}≥5KΩ ;VQ<VRT
reset output leakage current	I_{RQ}		0	1	uA	V_{RQ}=5V
Reset delay D:						
upper trigger threshold	V_{DT}		1.8		V	
lower trigger threshold	V_{DL}	0.2	0.4	0.6	V	
delay capacitor charging current	I_{Charge}	3	6	9	uA	V_D=0V
reset delay time	t_{rd}	10	15	20	ms	C_D=47nF
	t_{rd}		8		us	no capacitor on pins

1) Dropout voltage = VI-VQ (VI-VQ when VQ drops 100mV compared to the rated output voltage value when VI =13.5V).

6. Reset function

6.1、Reset threshold (V_{RT})

RQ must be externally connected to a pull-up resistor. Once the chip starts up, if the output voltage VQ falls below VRT, the chip will internally pull RQ low as a reset output.

This function can provide a reset low-level signal feedback to the MCU in case of chip output shorted to ground, thermal shutdown of the chip, or power supply undervoltage.

6.2、Reset response time (t_{rr})

After the output voltage VQ drops below VRT, RQ will be pulled low after a duration of t_{rr}.

6.3. Reset delay time (t_{rd})

Before the reset pin (RQ) is set high, an external capacitor is connected to the reset delay pin (D). At this point, D pin supplies a constant current (approximately around 6uA) to charge this external capacitor until the voltage at D pin exceeds the upper trigger threshold (V_{DT}) of the internal comparator. At that moment, R_Q will be set high.

If this pin is left floating, the default reset delay time is approximately 8 microseconds. The reset delay time, t_{rd}, is determined by the charging time of the external capacitor.

$$t_{rd} = \frac{C_D * 1.8V}{6}$$

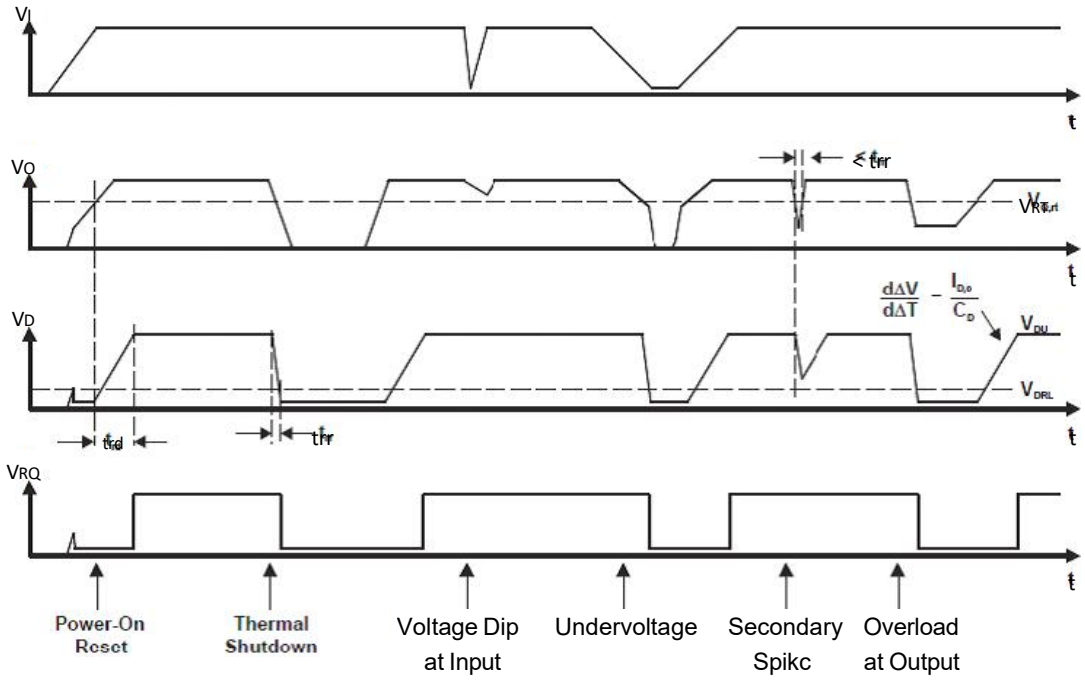


Fig.6-1 Reset Timing

7. Application information

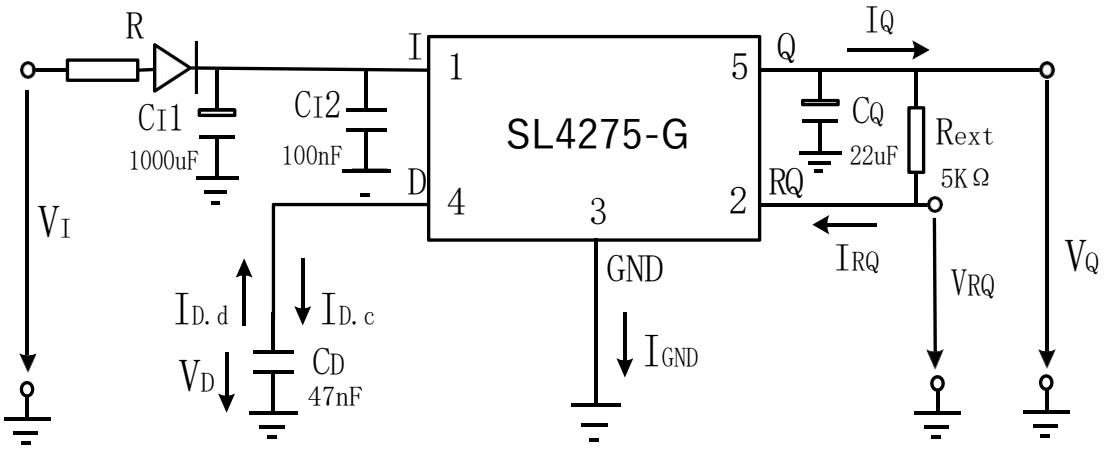


Fig.7-1 Application Circuit

8. Typical characteristic curve

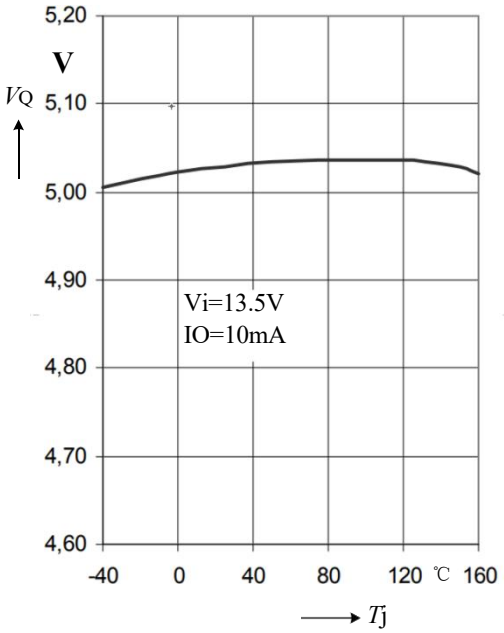


Fig.8-1 Output Voltage vs. Junction Temp

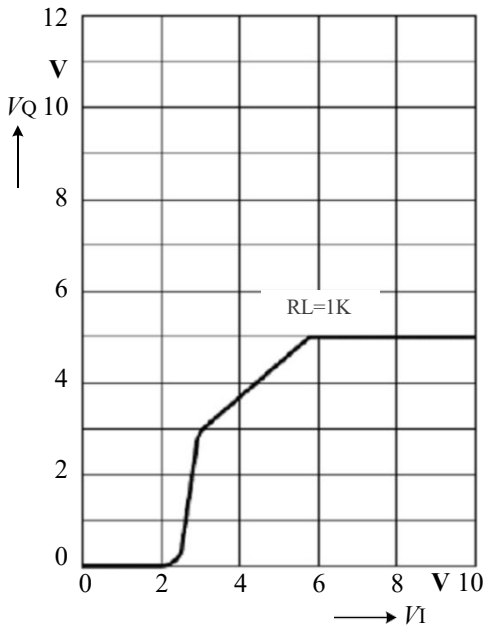


Fig.8-2 Output Voltage vs. Input Voltage

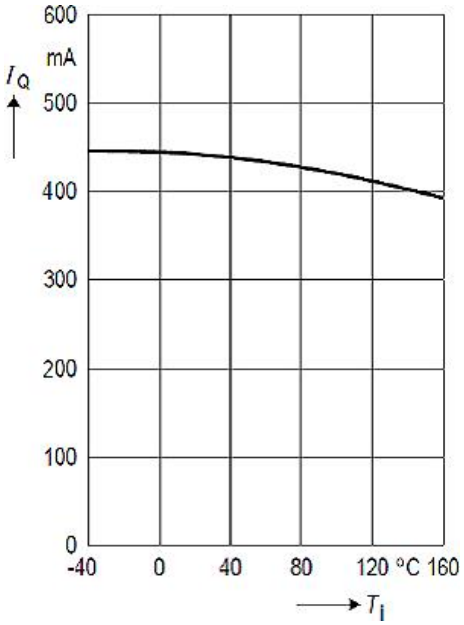


Fig.8-3 Output Current vs. Junction Temp

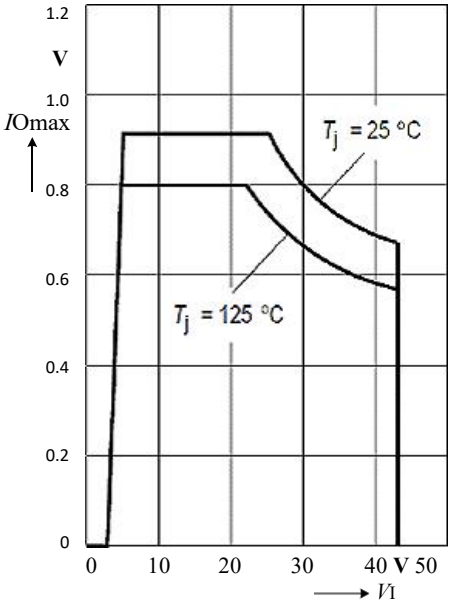


Fig.8-4 Output Current Limit vs. Input Voltage

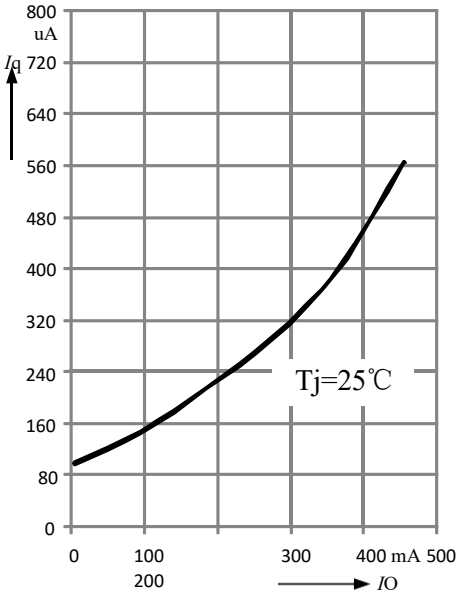


Fig.8-5 Quiescent Current vs. Output Current

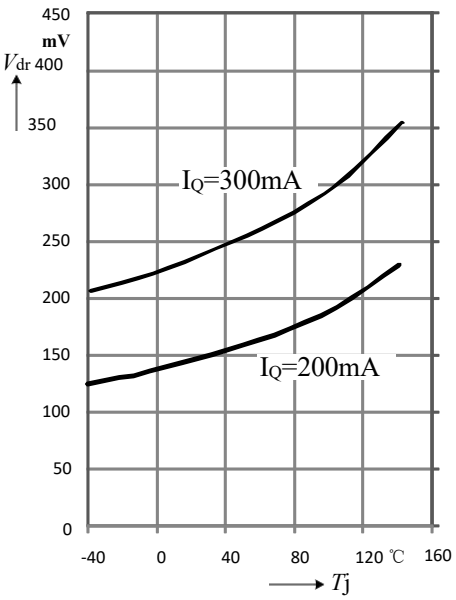


Fig.8-6 Dropout Voltage vs. Junction Temp

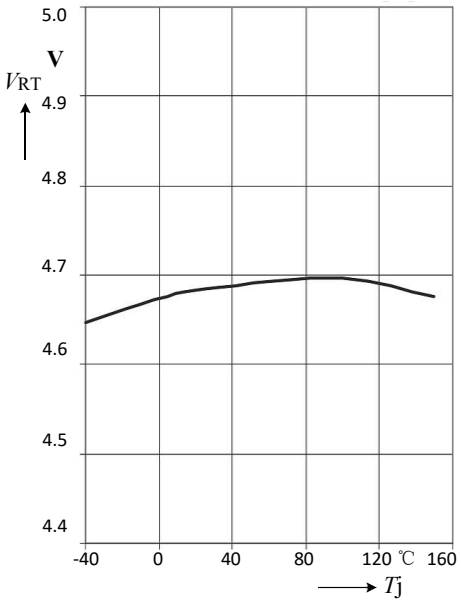


Fig.8-7 Reset Threshold vs. Junction Temp

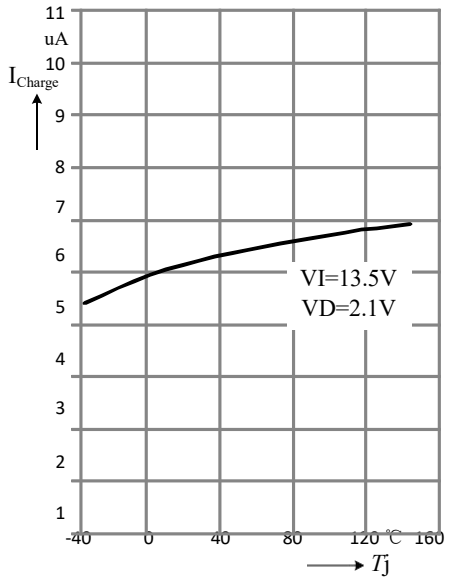
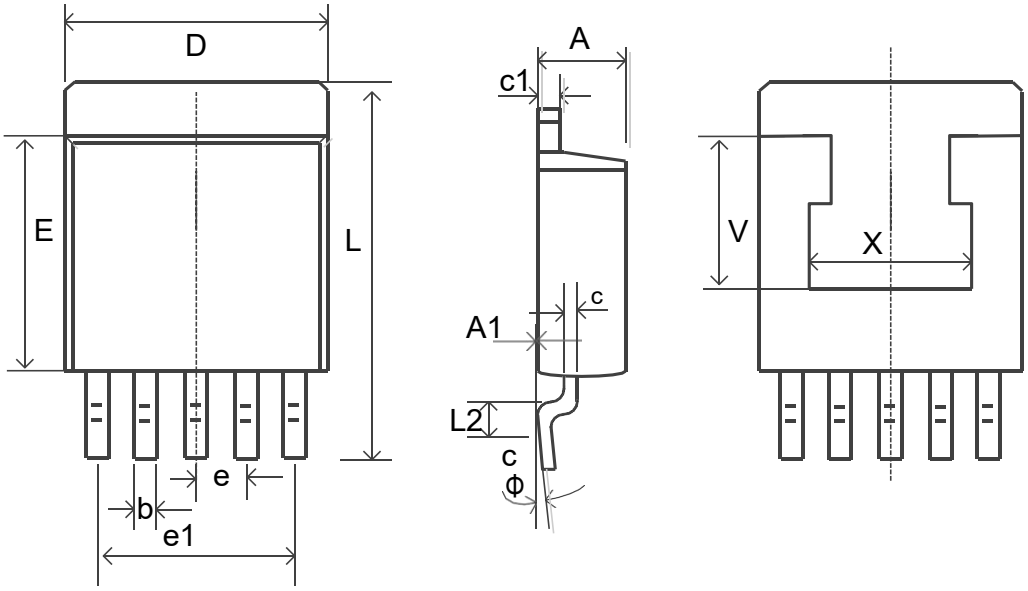


Fig.8-8 Reset Delay Charging Current vs. Junction Temp

9. Packaging dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.470	4.670	0.176	0.184
A1	0.000	0.150	0.000	0.006
b	0.710	0.910	0.028	0.036
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	9.880	10.18	0.389	0.401
E	8.200	8.600	0.323	0.339
e	1.700 TYP		0.067 TYP	
e1	6.700	6.900	0.264	0.272
L	15.14	15.54	0.596	0.612
L1	5.080	5.480	0.200	0.216
L2	2.340	2.740	0.092	0.108
Φ	0°	8°	0°	8°
V	6.250 REF		0.246 REF	
X	7.800 REF		0.307 REF	

Fig.9-1 TO263-5 Package