Versatile low dropout (LDO) regulators

1. Description

The SL4949 is a low-dropout (LDO) voltage regulator that outputs 5V. It integrates power-on reset functionality and input voltage monitoring internally.

The SL4949 provides a stable power supply voltage for microcontroller control systems, with a typical output current of up to 100mA. It can handle transient input voltages up to 42V, making it highly suitable for automotive electronic environments.

It supports Reset output for microprocessor logic control and includes Sense monitoring, which can provide a warning signal before issuing the reset signal. Proper use of Sense monitoring allows the microprocessor to take necessary processing steps before Reset halts its operation.

2. Features

- Operating voltage range: 5.5V to 42V
- Extremely low static current in standby mode: 80uA
- High precision standby output voltage: 5V ±1%
- Typical output current: 100mA
- Dropout voltage less than 0.4V
- Supports Reset output with adjustable reset delay time
- Features Sense voltage monitoring
- Over-temperature and short-circuit current limit protections
- RoHS compliant

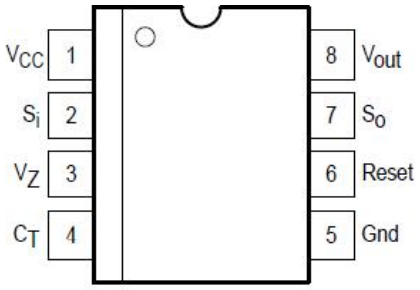
ESOP-8 SL4949S

SOP-8 SL4949

3. Applications:

- Automotive electronics
- Personal computers
- White goods appliances
- Industrial control products, electronic medical devices

4. Pin description



Top View

Fig.3-1 SL4949 / SL4949S Pin Layout

Pin	Symbol	Description
1	Vin	power input
2	Sense	voltage monitoring input
3	Vz	internal pre-processing module output
4	CT	reset delay setting
5	GND	ground
6	Reset	reset output
7	So	voltage monitoring output
8	Vout	regulated output
Exposed Pad		bottom heat sink, internally connected to GND

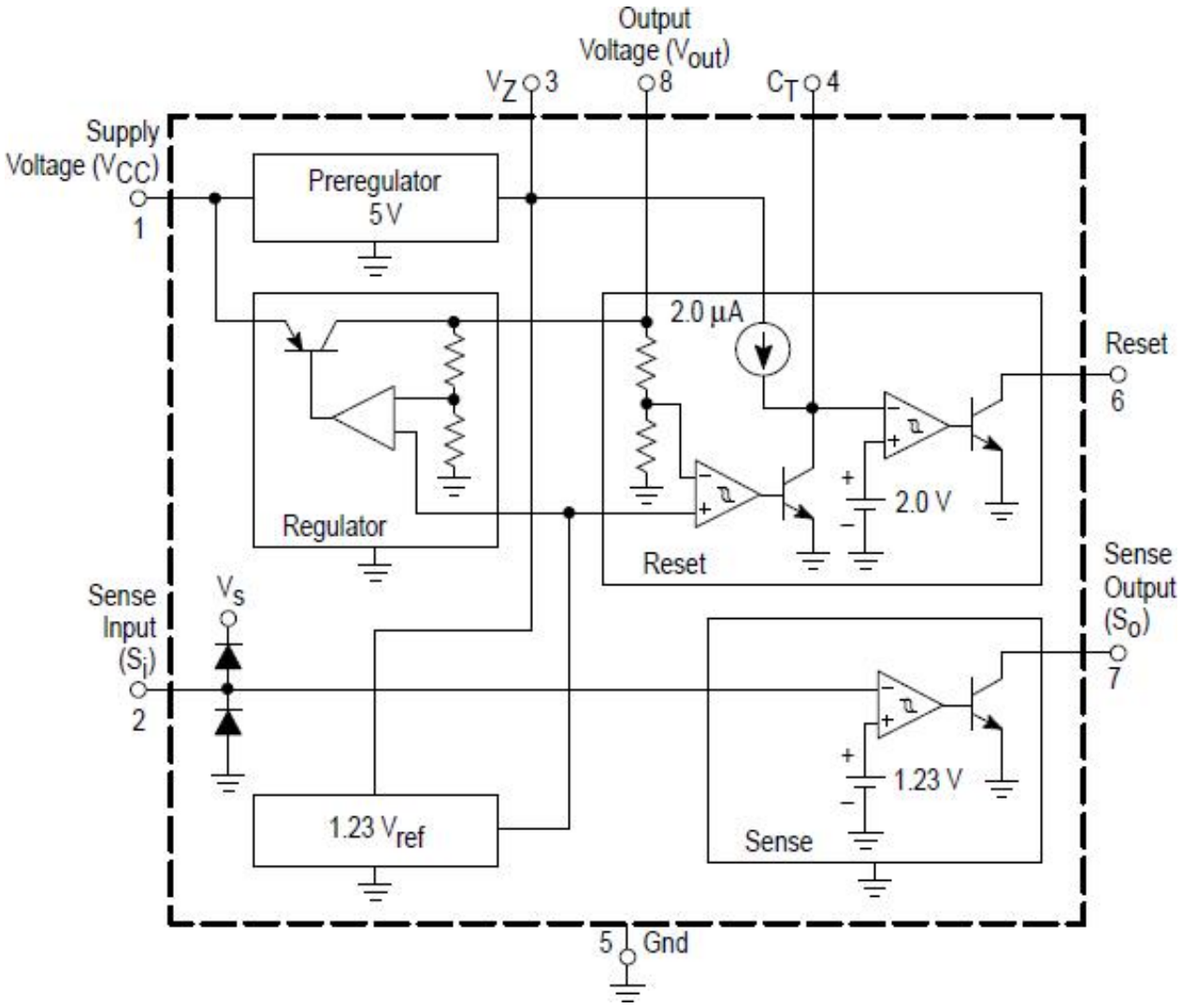


Fig.3-2 SL4949 / SL4949S Internal Diagram

5. Electrical parameters

Table 4.1 Maximum rated range (T_A = 25°C)

Parameter	Symbol	Numerical Value			Unit	Remark
		Min.	Typ.	Max.		
power supply voltage	V_{CC}	-	-	42	V	
output current	I_{out}			330	mA	internal current limiting
output voltage	V_{out}	4.95	5	5.05	V	
sense input current	I_{SI}	-	±1	-	mA	
sense input voltage	V_{SI}		V_{CC}			
internal pre-processing module output voltage	V_Z		5		V	
internal pre-processing module output current	I_Z		5		mA	
maximum junction temperature	T_j	-	-	150	℃	
storage temperature	T_{stg}	-40	-	150	℃	

Note: Prolonged exposure of the device to temperatures exceeding the maximum rated values listed above can adversely affect its reliability. These maximum rated values are absolute; exceeding any one parameter will result in permanent damage.

Table 4.2 Thermal resistance (T_A=25℃)

Parameter	Symbol	Numerical Value			Unit	Remark
		Min.	Typ.	Max.		
thermal resistance	R_{thJS}	-	-	200	K/W	SL4949
thermal resistance	R_{thJS}	50	-	90	K/W	SL4949S

Table 4.3 Electrical Characteristics (V_{CC} = 13.5V, T_A = 25° C)

Parameter	Symbol	Numerical Value			Unit	Remark
		Min.	Typ.	Max.		
output voltage	V_{OUT}	4.95	5.0	5.05	V	I_{out}=1.0mA
output voltage	V_{OUT}	4.9	5.0	5.1	V	6.0V<V_{CC}<28V 1.0mA<I_{out}<50mA
output voltage	V_{OUT}	4.9	5.0	5.1	V	V_{CC}=35V，t<1.0S 1.0mA<I_{out}<50mA
output current limit	I_{OUT}	100	-	330	mA	
voltage drop	V_{drop}	-	0.1	0.25	V	I_{out}=10mA
		-	0.2	0.40	V	I_{out}=50mA
		-	0.3	0.50	V	I_{out}=100mA
input voltage regulation	Reg_{line}	-	1.0	20	mV	6.0V<V_{CC}<28V I_{out}=1.0mA
load regulation	Reg_{load}	-	8.0	30	mV	1.0mA<I_{out}<100mA
current limit	I_{Lim}	105	-	330	mA	V_{out}=4.5V
		-	100	-	mA	V_{out}=0V
static current	I_{QSE}	-	80	100	uA	I_{out}=0.3mA, T_J<100℃
	I_Q		350	400	uA	I_{out}=100mA
Reset						
reset threshold voltage		Vout-0.7			V	
reset hysteresis threshold	$V_{Resth,\ hys}$	50	100	200	mV	@T_J=25℃
		50	-	300	mV	@T_J=-40～150℃
reset delay	t_{ResD}	55	100	180	ms	C_T=100nF， t_R≥100us
reset response time	t_{ResR}	-	5.0	30	us	C_T=100nF
reset output low level	t_{ResL}	-	-	0.4	V	R_{Reset}=10kΩ V_{CC}≥3.0V
reset leakage current	t_{ResH}	-	-	1.0	uA	V_{Reset}=5.0V
threshold voltage of delay comparator	V_{CTth}	-	2.0	-	V	

delay comparator threshold hysteresis	$V_{CTh,\ hys}$	-	100	-	mV	

SENSE

sense threshold	V_{SOth}	1.16	1.23	1.35	V	V_{SI}=1.5V～1.0V
sense threshold hysteresis	$V_{SOth,\ hys}$	20	100	200	mV	
sense output low level	V_{SOL}	-	-	0.4	V	V_{SI}≤1.16V V_{CC}≥3.0V R_{SO}=10kΩ toVout
sense output leakage current	I_{SOH}	-	-	1.0	uA	V_{SO}=5.0V V_{SI}≥1.5V
sense input current	I_{SI}	-1.0	0.1	1.0	uA	

PREREGULATOR

internal pre-processing module output voltage	V_Z	-	5.0	-	V	I_Z=10uA

6. Typical parameter curve

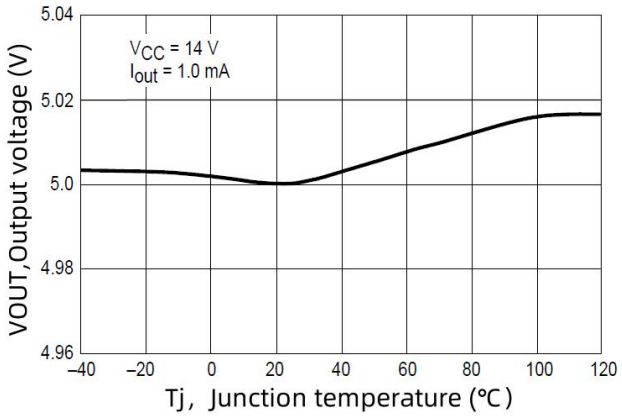


Fig.5-1 Output Voltage vs. Junction Temperature

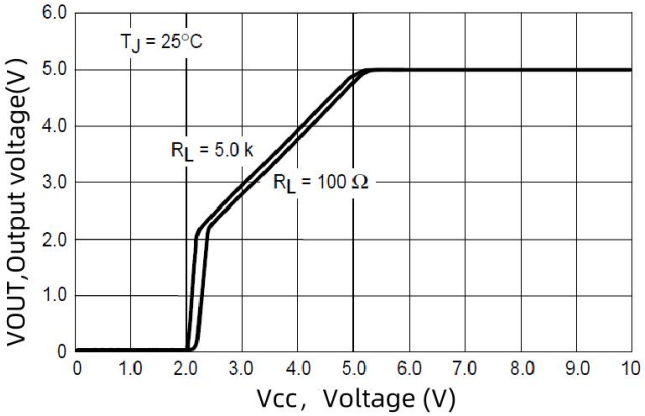


Fig.5-2 Output Voltage vs. Supply Voltage

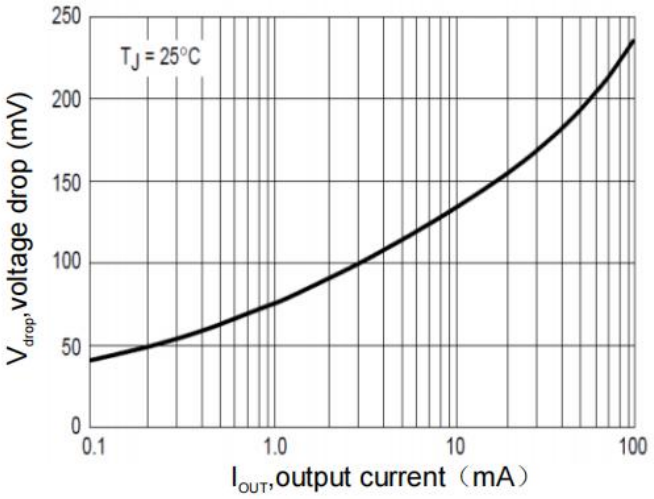


Fig.5-3 Voltage Drop vs. Output Current

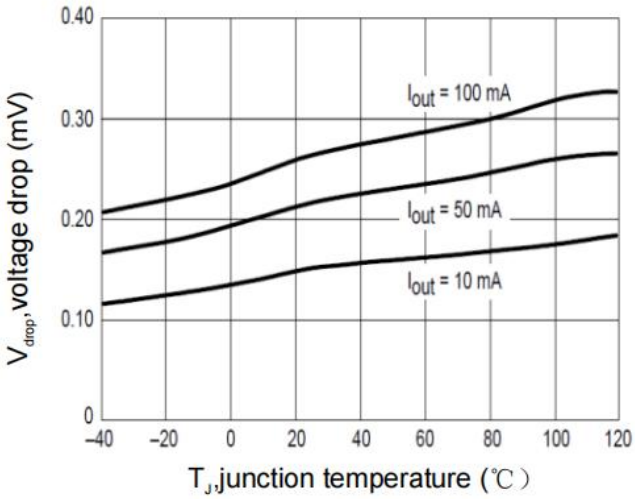


Fig.5-4 Voltage Drop vs. Junction Temp

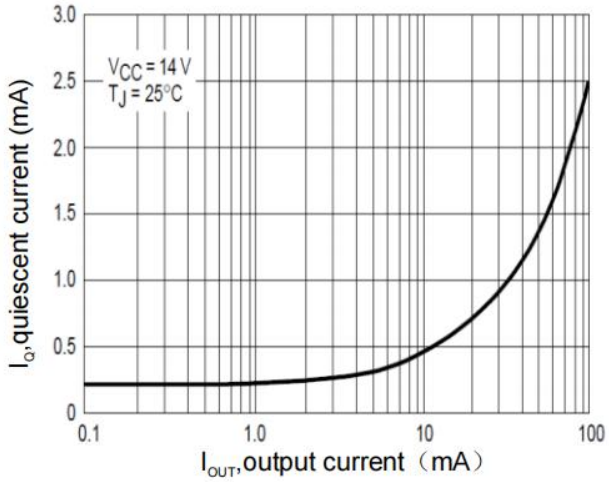


Fig.5-5 Quiescent Current vs. Output Current

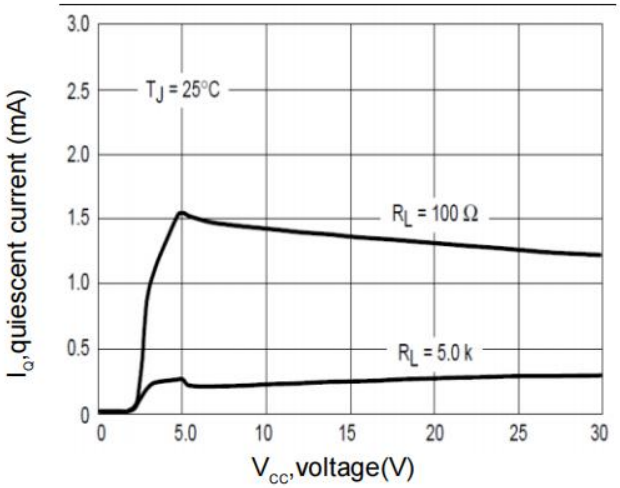


Fig.5-6 Quiescent Current vs. Input Voltage

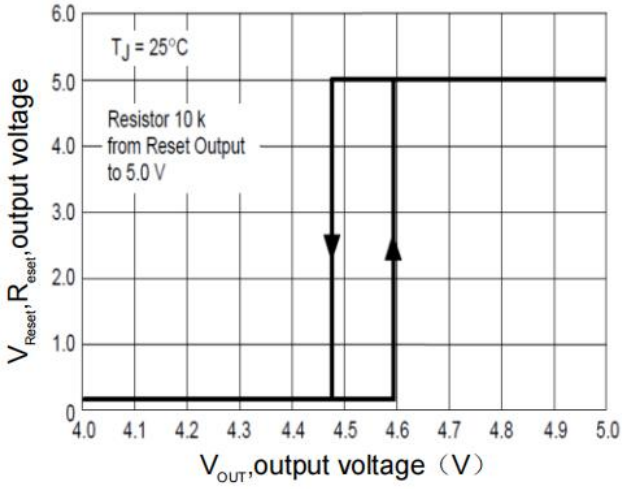


Fig.5-7 Reset Output Voltage vs. Output Voltage

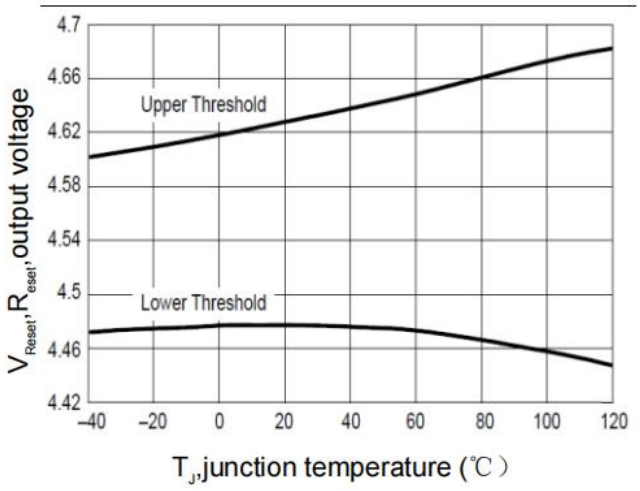


Fig.5-8 Reset Hysteresis Voltage vs. Junction Temp

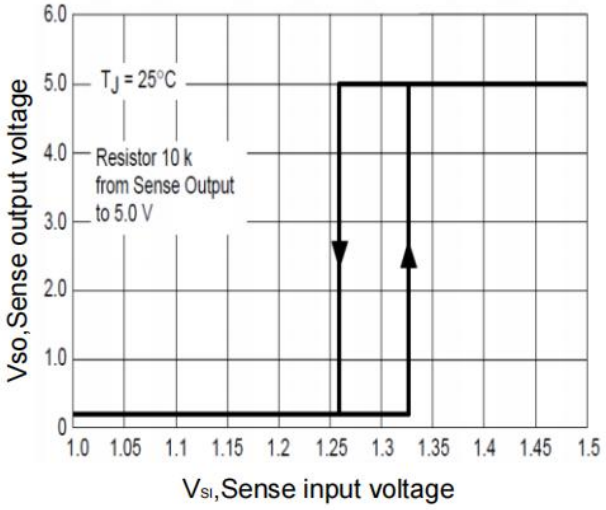


Fig.5-9 Sense Output Voltage vs. Sense Input Voltage

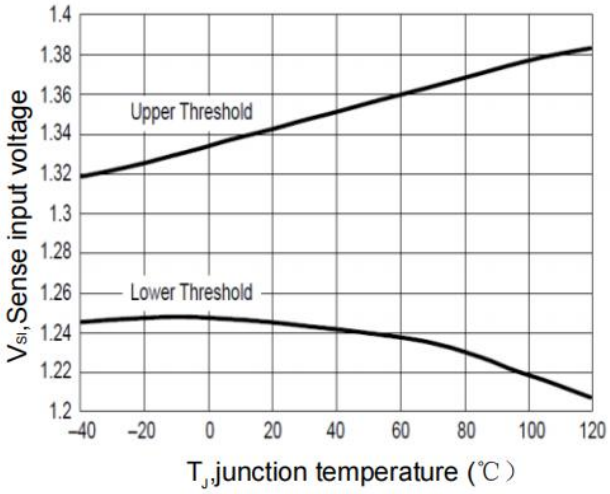
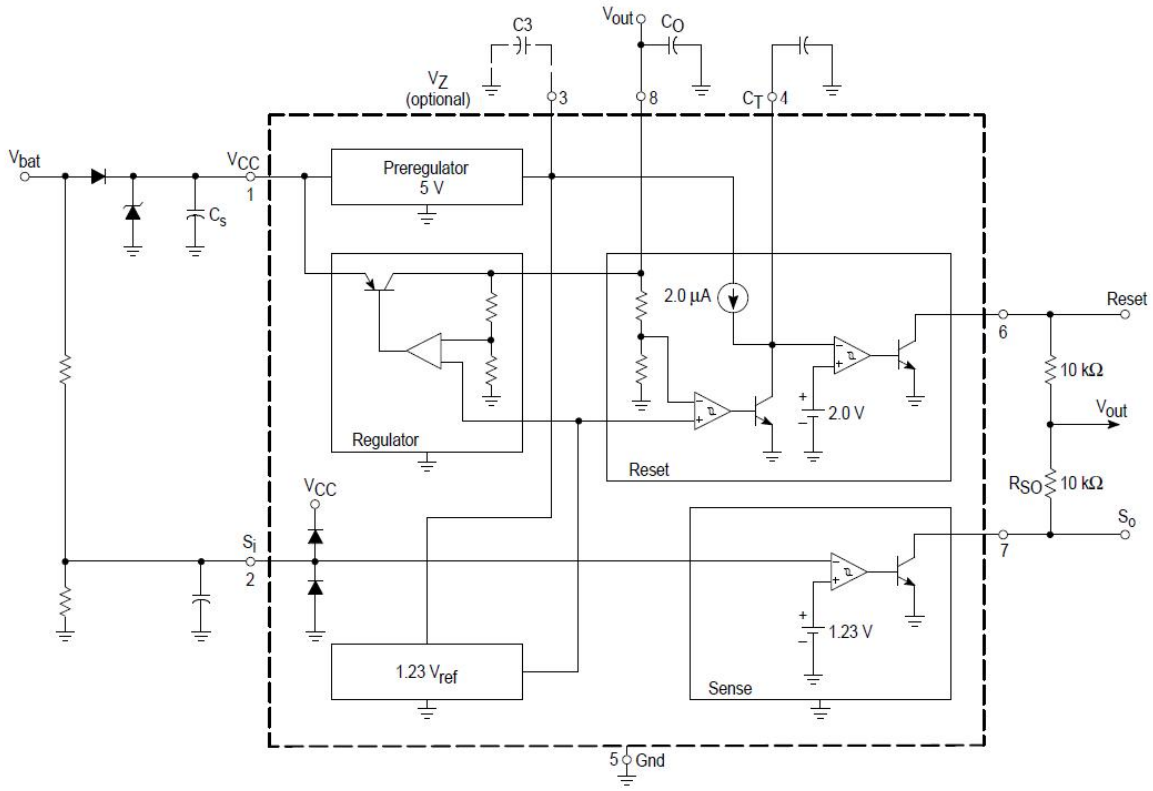


Fig.5-10 Sense Input Voltage vs. Junction Temp

7. Application

Transient supply voltage

Transient changes in power supply voltage may cause erroneous toggling of the Reset output signal. The chip exhibits strong immunity to interference when the power supply voltage is greater than 8.0V and transient changes exceed 100V/us, ensuring stable Reset output signals. However, when the power supply voltage drops below 8.0V and transient changes are less than 0.4V/us, it triggers erroneous toggling of the Reset output signal. To improve the chip's immunity to interference under low power supply voltages (<8.0V), a capacitor should be connected to Pin 3 (C3 ≤ 1.0uF), which also helps in reducing output noise.



Note: 1、$C_s \geqslant 1.0uF$，$C_o \geqslant 4.7uF$，$ESR < 10\Omega$；
2、recommend $C_o = C_s = 10uF$

Fig.6-1 SL4949 / SL4949S Typical Application Diagram

The SL4949 is a low-dropout (LDO) regulator designed to provide a stable 5V output voltage, suitable for microprocessor systems in automotive applications and other fields. Its modular design allows independent operation of each function.

Voltage regulator

The voltage regulator utilizes an independent vertical PNP transistor as the output device. This structure offers the advantage of minimal voltage drop at the output when the output current reaches 100mA. The output voltage remains stable when the input voltage is below 40V, ensuring that the SL4949 does not cease operation due to overvoltage pulses.

The curve of SL4949's output voltage changing with power supply voltage is shown in Figure 6-2.

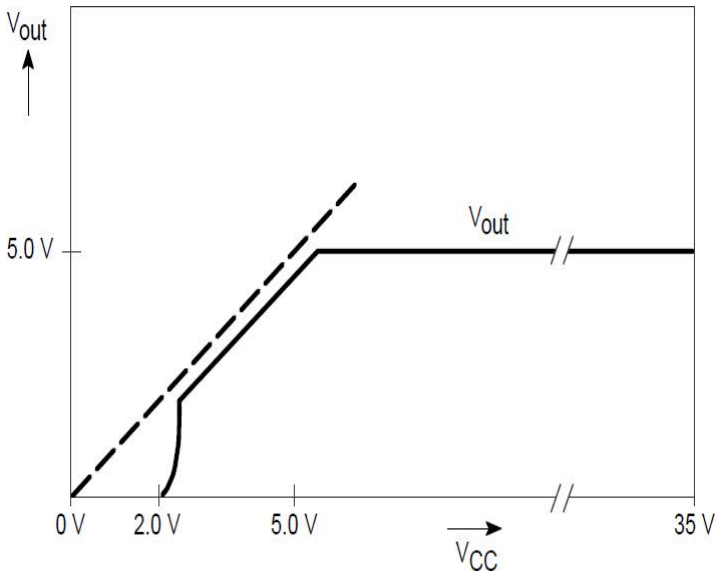


Fig.6-2 Output Voltage vs. Input Voltage

The SL4949 has a static current of less than 100uA. With the load disconnected, the SL4949 remains nearly unchanged as the input voltage increases, typically around 80uA.

Short-circuit protection: The SL4949 incorporates an internal current limit module set at 330mA.

Internal preprocessing module

To enhance the chip's transient immunity, the SL4949 features a pre-processing module internally, which supplies a stable 5V internal power source to other modules. The internal power supply voltage is directly accessible outside the chip via Pin 3 (Vz). Due to limited driving capability of the internal power supply voltage ($\leqslant$ 100uA), it is recommended not to use Vz as an output terminal.

When the supply voltage drops below 8V, to improve the chip's transient noise immunity, it is recommended to add a capacitor (100nF to 1.0uF) between Pin 3 and ground. Otherwise, Pin 3 should be left floating.

Reset circuit

The schematic diagram of the Reset circuit is shown in Figure 6-3.

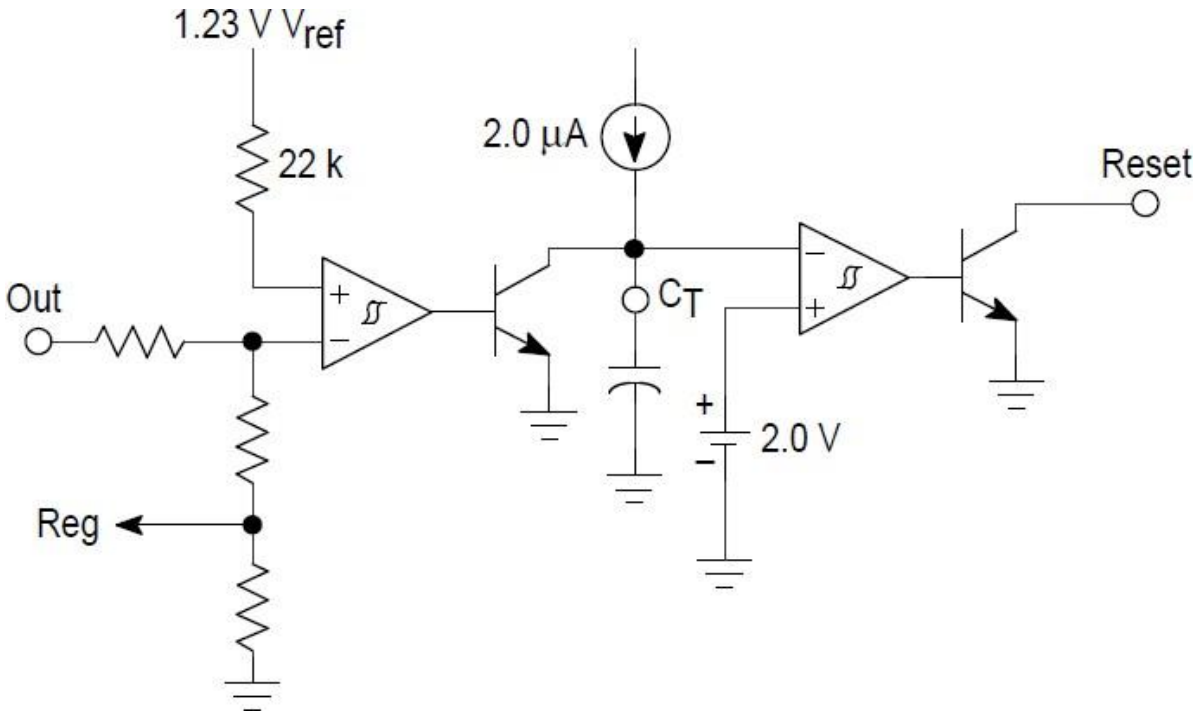


Fig.6-3 Reset Circuit

The reset circuit monitors the output voltage. It compares the output voltage with the internal Vref voltage, setting the reset threshold voltage to 4.3V.

The reset pulse delay time t_{RD} is determined by the charging and discharging time of capacitor C_T connected to pin 4, as shown in equation 6.1

$$t_{RD} = \frac{C_T \times 2.0V}{2.0uA} \qquad 6.1$$

According to equation 6.1, the response time of the reset circuit is determined by the discharge time of capacitor C_T, which is directly proportional to the capacitance of C_T. Increasing the response time can enhance the chip's noise immunity.

The rated reset delay time (Vout falling) is greater than 50us, with a typical Reset output waveform shown in Figure 6-4.

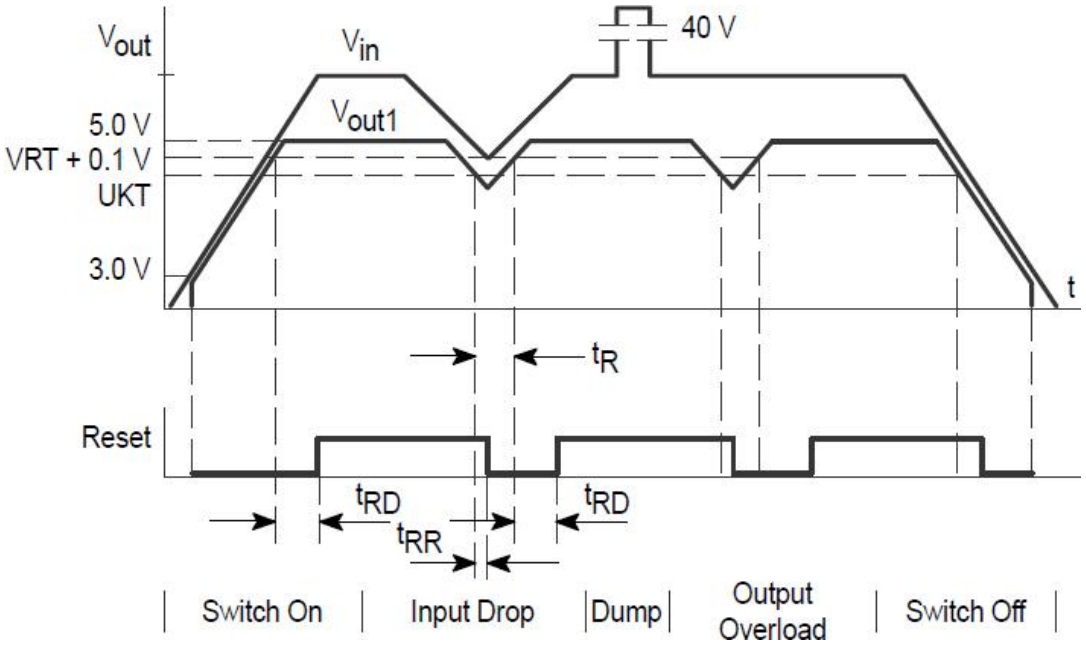


Fig.6-4 Typical Reset Output Waveform

Sense comparison circuit

Using a sense comparator circuit to monitor the power supply voltage enhances the flexibility of the sense comparator's application by employing an external voltage divider.

Before or after the activation of the chip's internal protection diode, sensibly utilize Sense to monitor input voltage, providing additional information to the microprocessor system, such as low voltage warnings.

8. SL4949 Package dimensions

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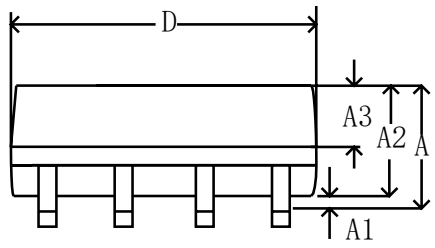
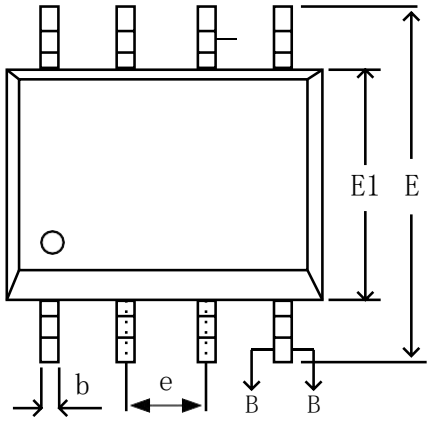
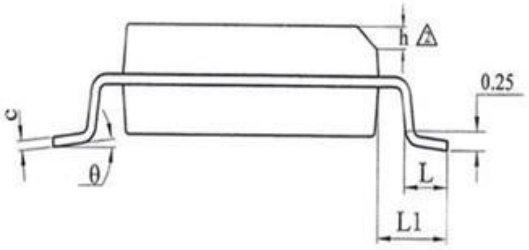
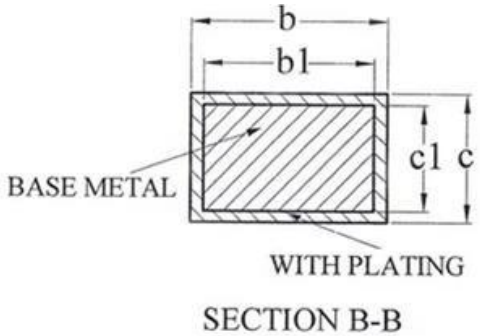




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.21	—	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05 BSC		
θ	0	—	8
L/F carrier size（mil）	80*80	90*90	95*130





SECTION B-B

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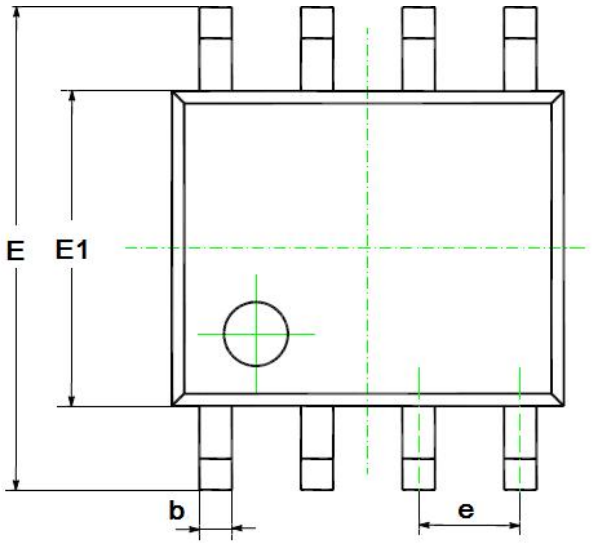
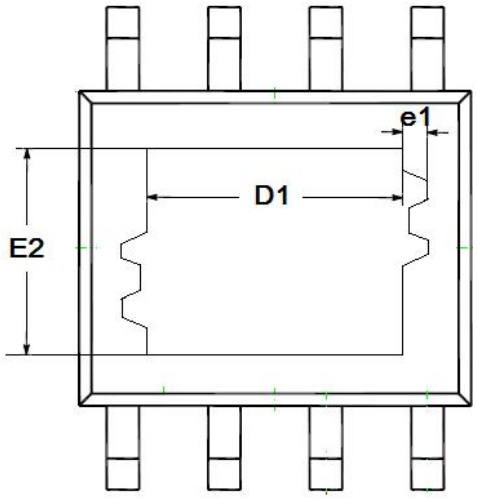
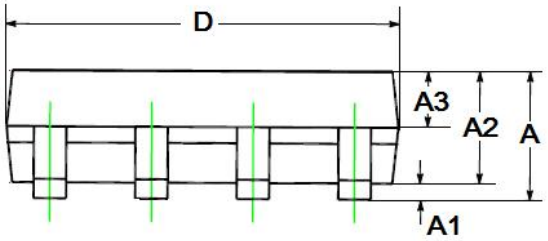


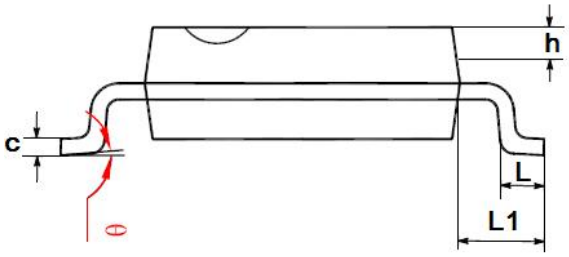
Top View



Bottom View



Side View



End View

Symbol	MM		
	Min.	Typ.	Max.
A	_		1.65
A1	0.05	_	0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	_	0.48
b1	0.38	0.41	0.43
C	0.21	_	0.25
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
D1	3.10REF		
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
E2	2.21REF		
e	1.27BCS		
e1	0.10REF		
h	0.25	_	0.50
L	0.50	0.60	0.80
L1	1.05BSC		
θ	0	_	8°