DC/DC Step-Down Voltage Regulator

Description

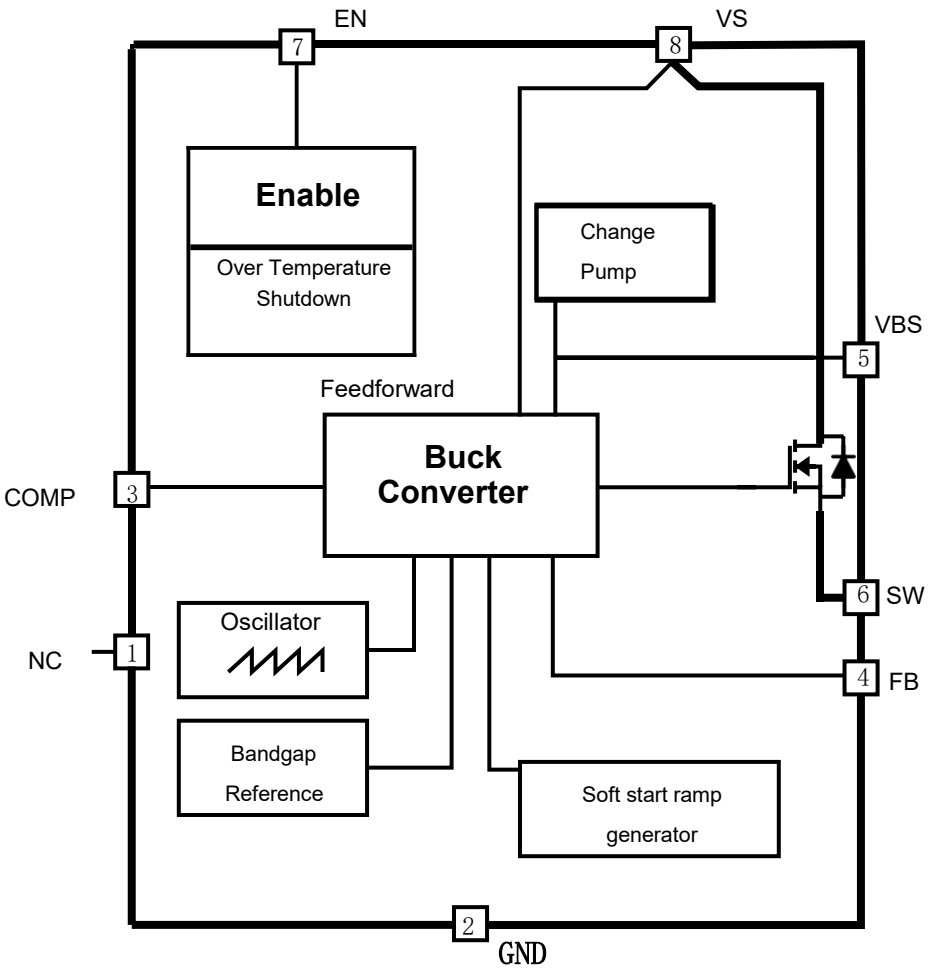
- SL8366 is a PWM buck DC/DC converter integrating a synchronous switch, housed in an ESOP-8 package with exposed pads. It features an adjustable output voltage with a reference feedback voltage of 600mV and operates over an input voltage range of 4.75V to 42V, making it suitable for a wide range of applications, designed for harsh automotive environments.
- The device operates nominally at 370kHz switching frequency, allowing the use of small inductors and capacitors to minimize output ripple and PCB footprint.
- SL8366 incorporates several protection features including cycle-by-cycle current limiting, thermal shutdown, and input undervoltage lockout. It includes an enable switch function where power consumption is below 10μA when disabled, ideal for battery-powered systems.
- The voltage regulation loop offers excellent line and load transient responses. Stability of the regulation loop is ensured through the use of an external compensation network. The compensation circuit, combined with voltage-mode regulation and feed forward control path, ensures outstanding power noise suppression performance. On startup, integrated soft-start functionality limits surge current peaks and prevents voltage overshoots.

Feature

- 1.8A Buck Regulator, Adjustable Output Voltage
- ±2% Output Voltage Accuracy (±4% over full load current range)
- Integrated MOSFET
- PWM Regulation with Feedforward
- Input Voltage Range: 4.75V to 42V
- Fixed Switching Frequency of 370KHz
- Very Low Shutdown Quiescent Current (<10uA)
- Integrated Soft-Start and Input Undervoltage Lockout
- RoHS Compliant

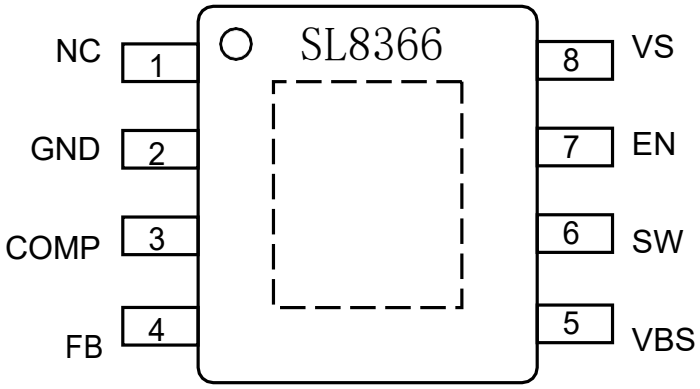
ESOP-8

Block Diagram



SL8366 Block Diagram

Pin configuration and function

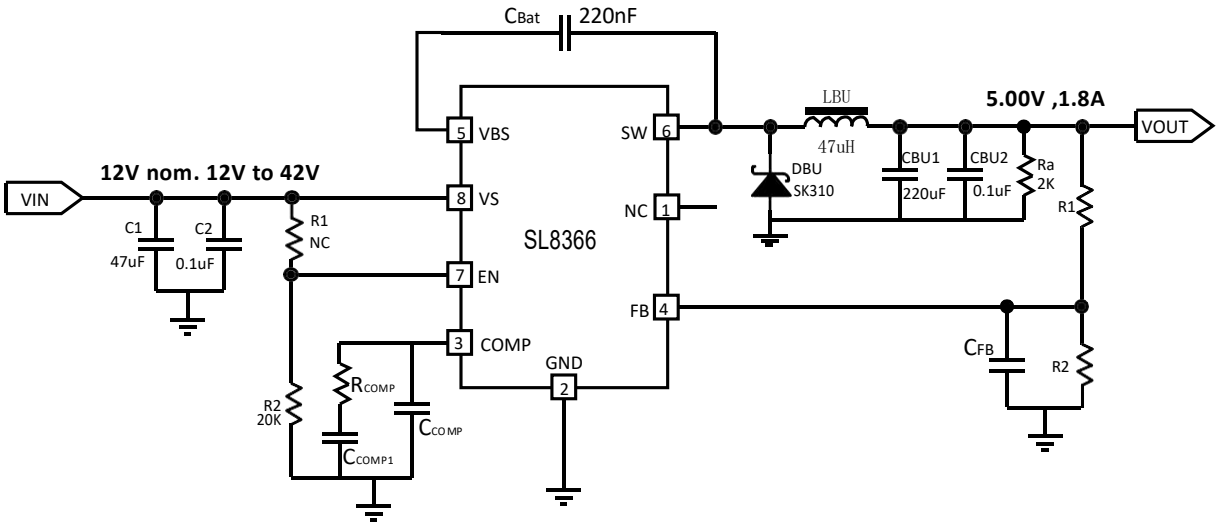


Pin Arrangement

Table Pin Function

Pin NO.	Pin Name	Description
1	NC	open circuit
2	GND	ground
3	COMP	compensation input frequency compensation for regulating loop stability. connected to compensation RC network.
4	FB	feedback input connected through a voltage divider to the output capacitor.
5	VBS	boost module power input connected via a bootstrap capacitor between this pin and SW pin.
6	SW	buck switch output source terminal of the power DMOS transistor, directly connected to the cathode of the freewheeling diode and inductor.
7	EN	enable input active high with internal pull-down current.
8	VS	power
exposed pad		connected to the heatsink area and GND.

Typical application circuit



The output voltage of SL8366 can be adjusted using a voltage divider connected to the feedback pin FB. The minimum current through the voltage divider should be 300uA, therefore the maximum value of R2 is calculated as:

$$R_2 \leq V_{FB}/I_{R2} \text{ --> } R_2 \leq 0.6V/300\mu A = 2k\Omega$$

To obtain the desired output voltage V_{OUT}, R1 is calculated using formula 4.1 (ignoring the small input current of FB pin)

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{FB}} - 1\right) \qquad 4.1$$

it is recommended to add a 0.5 nF capacitor near the FB pin.

Absolute Maximum Rating（Unless otherwise specified, T_j = -40°C to +150°C; all voltages are referenced to ground.）

Parameter	Symbol	Min	Max	Unit	Condition
Voltage					
compensation input feedback input	V_{COMP}	-0.3	5.5	V	
			6.2	V	T<10s[2])
boost driver	V_{FB}	-0.3	5.5	V	
power input	V_{VBS}	-0.3	5.5	V	
buck switch	V_{SW}	-2.0	VS+0.3	V	
enable input	V_{EN}	-0.3	45	V	
power input	V_{VS}	-0.3	45	V	
Temperature					
junction temperature	T_j	-40	150	℃	
storage temperature	T_{stg}	-40	150	℃	
ESD					
ESD withstand voltage	V_{ESD}	-2	2	kV	HBM[3])
voltage withstand to ground	V_{ESD}	-500	500	V	CDM[4])
pin-to-ground withstand voltage	V_{ESD}	-750	750	V	CDM[4])

[1])Not intended for product testing, as determined by design.

[2])Extended exposure of the device to extreme conditions (>10s) may affect device reliability.

[3])ESD withstand voltage HBM according to EIA/JESD22-A114B (1.5kΩ, 100pF).

[4])ESD withstand voltage, charged device model "CDM" EIA/JESD22-C101 or ESDA STM5.3.1.

Note:

1) Conditions exceeding the limits specified in the above list may cause permanent damage to the device. Prolonged exposure of the device to extreme conditions can impact its stability.

2) Integrated protection features are designed to prevent IC damage under improper operating conditions. Improper conditions refer to those beyond the normal operating range. Protection features are not intended for repeated improper operation.

Operating conditions

5.2 Table

Parameter	Symbol	Min	Max	Unit	Description
power supply voltage	V_S	4.75	42	V	
output voltage adjustment range	V_{CC}	0.60	16	V	
step-down inductor	L_{BU}	18	56	uH	
step-down capacitor	C_{BU1}	33	-	uF	
step-down capacitor ESR (equivalent series resistance)	ESR_{BU1}	-	0.3	Ω	1）
junction temperature	T_j	-40	150	℃	

1） Compensation circuit requirements are detailed in Chapter 9.

Explanation: Within the operating conditions range, the IC operates as described in the circuit description. Electrical characteristics are specified for conditions given in the relevant electrical characteristics table.

Thermal resistance coefficient

5.3 Table

Parameter	Symbol	Min	Max	Unit	Description	Parameter
PN junction to case 1）	R_{thJC} 1）	-	10	12	K/W	-
PN junction to ambient 1）	R_{thJA} 1）	-	52	-	K/W	2）

1） Not for product testing, as determined by design.

2） According to JEDEC JESD52-1, -5, -7, testing values under natural convection conditions on a 2s2p FR4 PCB. PCB dimensions are 76.2×114.3×1.5mm³, with 2 internal copper layers (2 x 70μm Cu). Heat dissipates through the thermal pad beneath the chip, conducting to the first copper layer.

Buck regulator

Description

The buck regulator consists of several functional modules, detailed as follows: oscillator, regulator, protection features, gate driver, and internal MOSFET.

Regulator Module:

Oscillator generates a sawtooth signal, provided to the PWM comparator and Schmitt trigger 1.
Error amplifier compares feedback signal with reference voltage. Feedback pin connects to an external resistor divider. Soft-start function is included in the ramp generator, positioned between the reference voltage source and error amplifier. Upon device initialization, it generates a defined ramp signal. Ramp generation occurs if the buck drive voltage (VVBS) charges an external capacitor.

Compensation circuit connects to the output of the internal error amplifier via the COMP pin.
PWM comparator generates pulse width modulation (PWM) signal by comparing error amplifier output with the sawtooth signal from the oscillator.

Protection Function Module:

Protection function comprises fault trigger, NOR1 gate, and PWM trigger.
Fault trigger gathers fault signals such as overcurrent shutdown of internal MOSFET, output overvoltage shutdown, and over-temperature shutdown.

Overcurrent shutdown signal is generated by the OC comparator. It detects voltage across an internal shunt resistor. If current exceeds the reference value, pulses are shut off and MOSFET is turned off.Bootstrap undervoltage shutdown is generated by the bootstrap drive excitation source's undervoltage comparator, which compares bootstrap capacitor voltage with a reference level. If bootstrap capacitor voltage is too low, pulses are shut off, and MOSFET is turned off.

If output voltage exceeds the reference value, pulses are shut off, and MOSFET is turned off. An internal temperature sensor monitors device temperature; if junction temperature exceeds 150°C, MOSFET shuts off.Fault trigger resets NOR1 gate and clears any fault signal. This closes NOR1 gate and shuts off pulses.

Bootstrap capacitor monitor connects directly to NOR1 gate.PWM pulses are transmitted through NOR1 gate. If any of the aforementioned fault conditions occur, this gate circuit closes and pulses immediately shut off.PWM trigger is set by NAND2, with inputs from clock of Schmitt trigger 1 and output of NOR1. PWM trigger is reset by output of NOR1.

Internal Power Module

The gate driver module consists of a gate drive circuit, PWM signal inverter, and gate drive circuit power supply. The gate drive circuit power supply is connected to capacitor CBOT via pin VBS (as shown in Figure 4-2). It integrates a charge pump to support gate drive in scenarios of low input voltage, minimal difference between input and output voltage, or during startup. To minimize radiation, the charge pump is disabled if the input voltage is sufficiently high to charge the bootstrap capacitor.

Operating Modes

PWM pulses are voltage-controlled. The error amplifier and PWM comparator compare the oscillator sawtooth signal with the feedback voltage, generating PWM pulses. Pulse-width modulation adjusts the feedback voltage (at pin FB for adjustable voltage models) to approximate the reference voltage (0.6V).

With input voltage ranging from 8.0V to 42V, the integrated feedforward path provides rapid linear transient response (feedforward detects input voltage and adjusts promptly to ensure output stability before input fluctuations propagate to the output). To achieve stable output voltage, pulse skipping mode is utilized under conditions of low duty cycle (light load to no load and/or high input voltage).

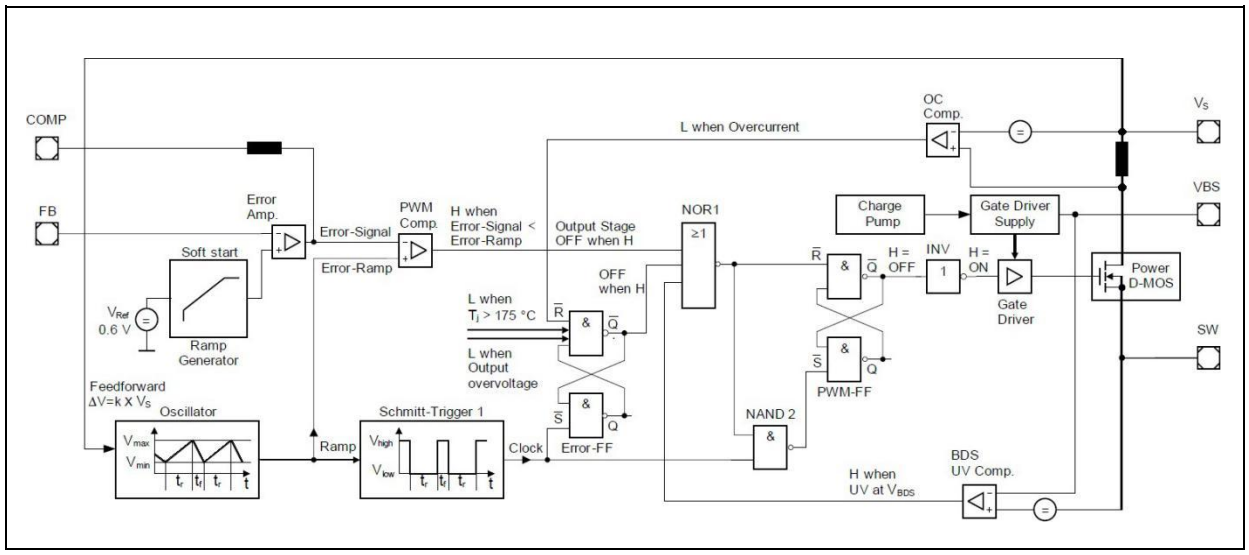


Figure1 Buck Regulator Module Block Diagram

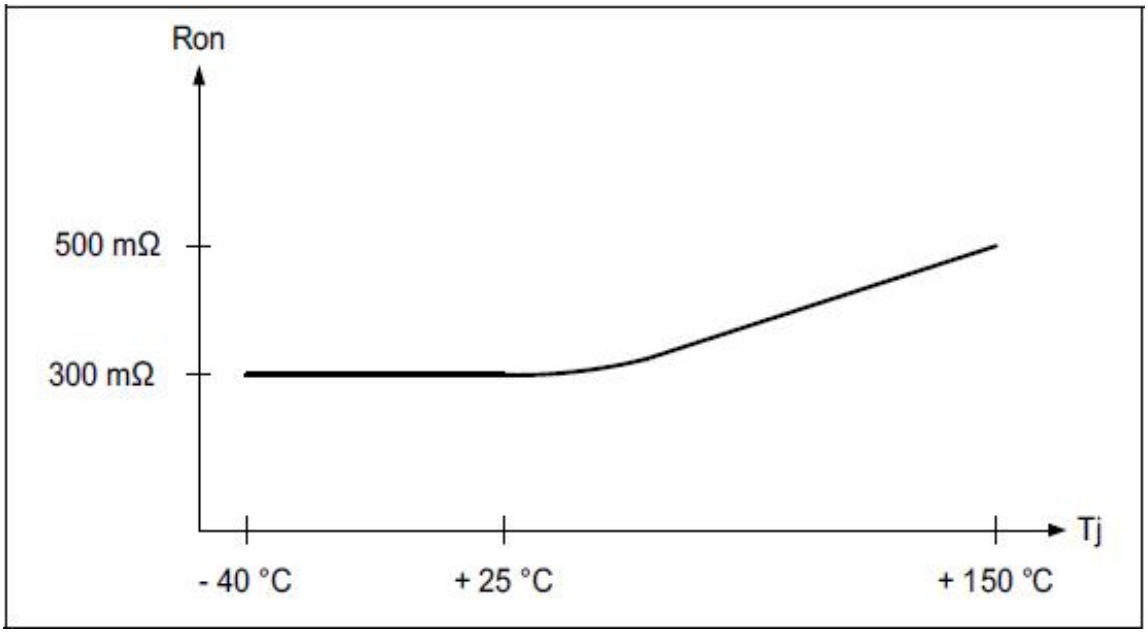


Figure2 The relationship between the on-resistance of power transistors and temperature

Electrical characteristics（Unless otherwise specified,V_s=6.0V～40V, T_j = -40°C to +150°C; all voltages are referenced to ground.）

Parameter	Symbol	Min	Typ	Max	Unit	Condition
output voltage	V_{FB}	0.588	0.6	0.612	V	V_{EN}=V_S,FB=V_{OUT} V_S=12V，0.1A<I_{OUT}<1.0A
	V_{FB}	0.576	0.6	0.624	V	V_{EN}=V_S,FB= V_{OUT} V_S=12V 1mA< I_{OUT} <1.8A
minimum output load	$I_{CC,MIN}$	1.5			mA	V_{OUT} >3V
		5			mA	V_{OUT} >1.5V
		10			mA	V_{OUT} >0.6V
feedback input current	I_{FB}	-1	-0.1	0	uA	V_{FB}=0.6V
power MOSFET on-resistance	R_{on}		130		mΩ	Testing under 300mA conditions
current transients rise/fall time	t_r		50		ns	I_{OUT} =1A 1)
peak output current	I_{SWC}	2.2		3.6	A	
bootstrap undervoltage shutdown threshold	$V_{VBS,off}$	V_{SW}+ 3.3			V	Bootstrap voltage drop
charge pump current	I_{CP}	2			mA	V_S=12V，V_{SW}=V_{VBS}=GND
charge pump shutdown threshold	V_{SW}-V_{VBS}			5	V	（V_{SW}-V_{VBS}）up
maximum duty cycle	D_{MAX}			95	%	1)
soft-start slope	t_{start}	350	500	750	us	V_{FB} rising from 5% to 95%
input undervoltage shutdown threshold	$V_{S,off}$	3.75			V	V_S down
input startup threshold	$V_{S,on}$			4.75	V	V_S up
input undervoltage shutdown hysteresis	$V_{S,hyst}$	150			mV	

1）Refer to "Table 5.2 Operating Conditions".

Enable control module and over-temperature protection

Description

By enabling the EN pin, the device can be set to a shutdown state, reducing current consumption to below 10μA. The enable function includes an integrated pull-down current to ensure internal module shutdown and power switch closure when pin EN is floating.

The chip integrates over-temperature protection, which shuts down the power switch when overheating occurs. The typical shutdown threshold is 160°C, with a minimum of 150°C. After cooling down, the IC automatically resumes operation. Over-temperature protection is an integrated safeguard that promptly shuts down the chip to prevent damage when temperatures exceed safe limits. The over-temperature protection module does not shut down the chip during normal operation.

Electrical characteristics

（Unless otherwise specified,V_s=6.0V～40V, T_j = -40°C to +150°C; all voltages are referenced to ground.）

Parameter	Symbol	Min	Typ	Max	Unit	Condition
static current in shutdown state	$I_{q,OFF}$		8	10	uA	V_{EN}=0.8V； T_j<105℃；V_s=16V
static current in startup state	$I_{q,ON}$			550	uA	V_{EN}=5V； I_{CC}=0mA； V_s=16V； FB=VSW
	$I_{q,ON}$			550	uA	V_{EN}=5V； I_{CC}=1A；V_s=16V； FB=VSW
enable high active	$V_{EN,hi}$	1	1.08	1.15	V	
enable low active	$V_{EN,lo}$	0.7	0.78	0.85	V	
enable hysteresis	$V_{EN,HY}$	50	200	400	mV	
enable high input current	$I_{EN,hi}$			1	uA	V_{EN}=16V
enable low input current	$I_{EN,lo}$		0.1	1	uA	V_{EN}=0.5V
over-temperature shutdown	$T_{j,sd}$		150		℃	
over-temperature hysteresis	T_{j,sd_hyst}		15		℃	

1) The above are design parameters, not specific to product testing.

Oscillator

Description

The oscillator provides a fixed frequency to the chip. The power switch is turned on and off at a fixed frequency. The duty cycle is derived from this frequency, and some protection functions are synchronized with it. The amplitude of the internal sawtooth signal used to generate PWM is proportional to the input supply voltage.

（Unless otherwise specified,V_s=6.0V～40V, T_j = -40°C to +150°C; all voltages are referenced to ground.）

Parameter	Symbol	Min	Typ	Max	Unit	Description
oscillation frequency	f_{osc}	330	370	420	kHZ	

Application Information

Note: The following information is for reference only and should not be considered a guarantee of specific functions, conditions, or qualities of the device.

Frequency Compensation

Connecting an RC circuit between the COMP pin and GND can improve the stability of the error amplifier's output. It is recommended to use a ceramic capacitor C_{OMP} = 22nF and resistor R_{COMP} = 22kΩ. Minor adjustments to the compensation network can optimize its stability for different application requirements, such as varying types of decoupling capacitors (ceramic or tantalum capacitors). The stability of the control loop heavily relies on the compensation network. Leaving the COMP pin floating may result in unstable operation of the chip.

Decoupling tantalum capacitor CBU1

Ceramic decoupling capacitor CBU effectively optimizes the control loop. To maintain stability and accommodate the load of tantalum capacitors (with ESR < 300mΩ), an additional compensation capacitor C_{COMP2} is required between the COMP pin and GND, as per Equation 9.1:

$$C_{COMP2} = C_{BU} * ESR\ (C_{BU}) / R_{COMP} \qquad 9.1$$

Where C_{COMP2} should be less than 5nF.

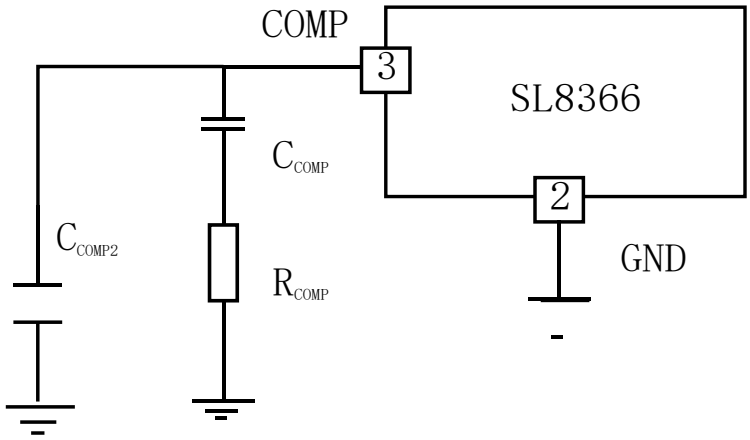


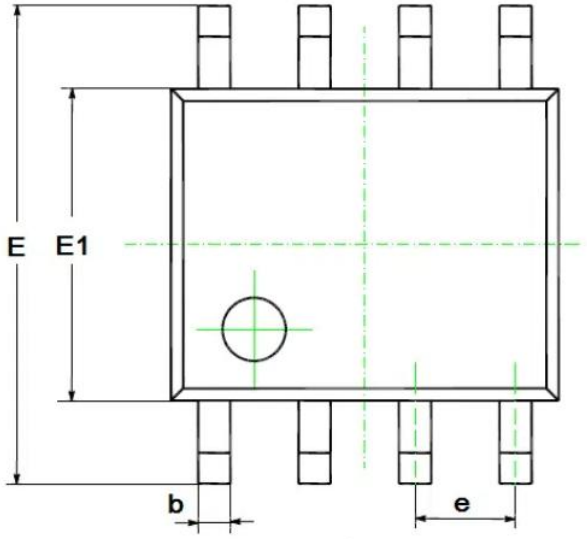
Figure 9-1 compensation circuit

Freewheeling Diode

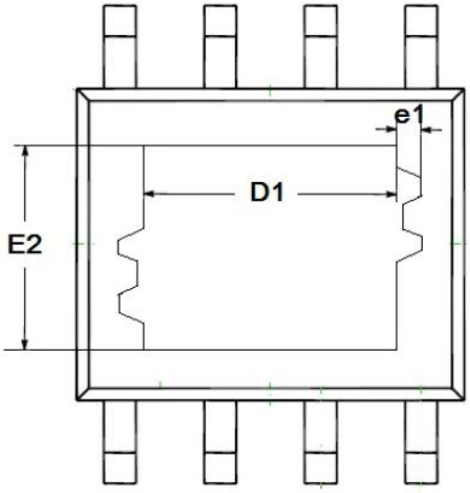
A Schottky freewheeling diode effectively minimizes losses and provides a fast recovery path. Disconnecting this diode during operation may damage the chip. It is recommended to use a 3A/60V Schottky diode.

SL8366 Package

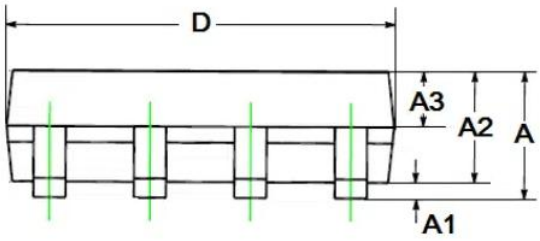
eSOP8, 8LEAD



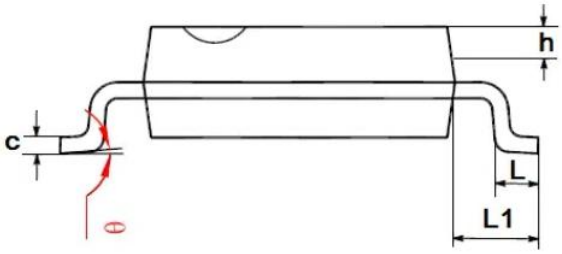
Top view



Bottom view



Side view



End view

Symbol	mm		
	Min	Typ	Max
A	–	–	1.65
A1	0.05	–	0.15
A2	1. 30	1. 40	1. 50
A3	0.60	0.65	0.70
b	0.39	–	0.48
b1	0.38	0.41	0.43
c	0.21	–	0.25
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
D1	3.10REF		
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
E2	2.21REF		
e	1.27BCS		
e1	0.10REF		
h	0.25	–	0.50
L	0.50	0.60	0.80
L1	1.05BSC		
θ	0	–	8°