Pulse width modulation (pwm) circuit

Description

UC3843AN is a current-mode PWM integrated circuit designed for switching power supplies. It offers significant advantages over voltage control methods in aspects such as load response and linearity of adjustment.

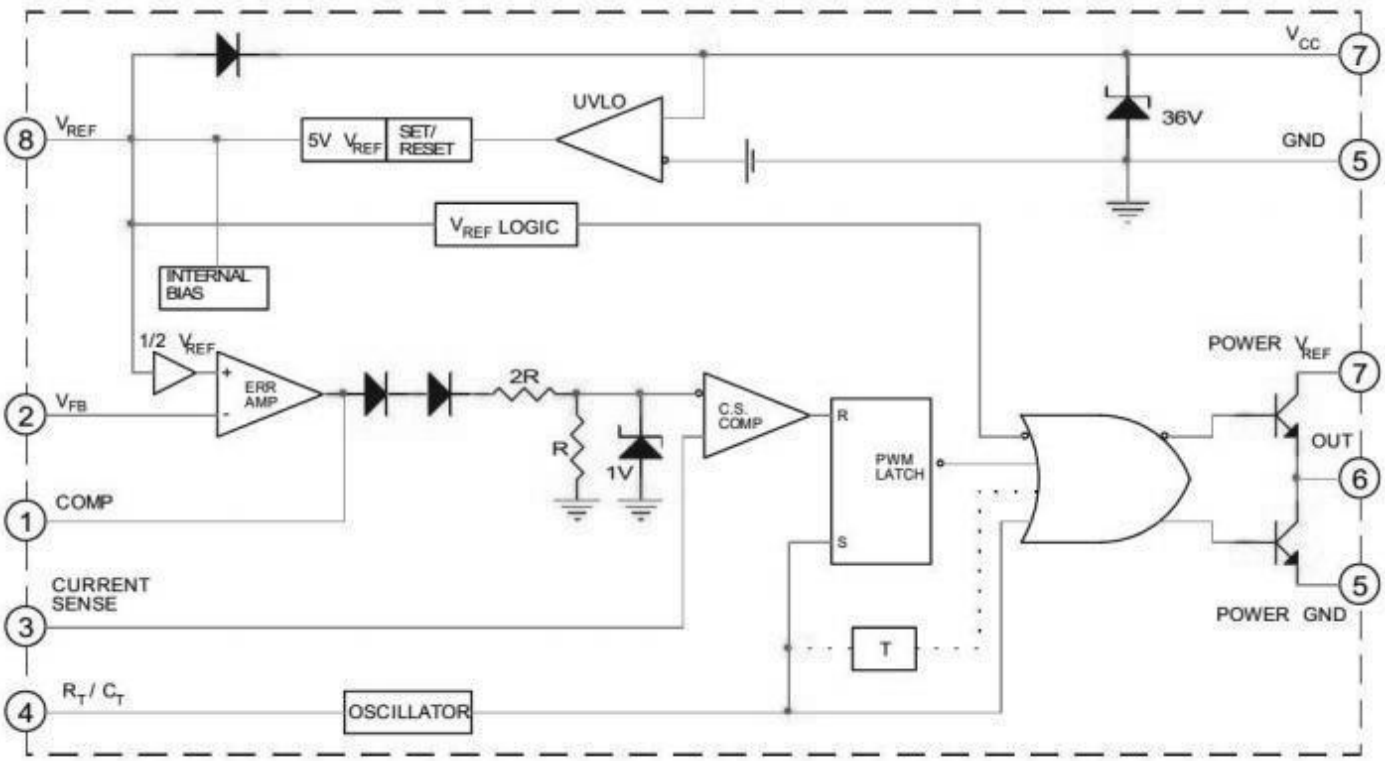
Feature

- Includes undervoltage lockout circuit
- Low startup current (typical value is 70uA)
- Stable internal reference voltage source
- High-current totem-pole output (drive current up to 1A)
- Operating frequency up to 500kHz
- Automatic feedback compensation circuit
- Double pulse suppression
- Strong load response characteristics

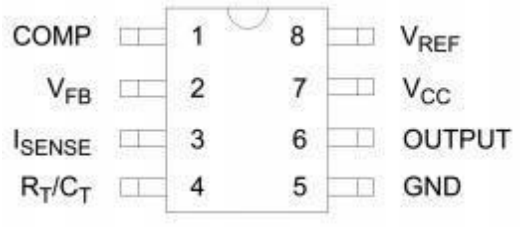
Pakage type：

SOP-8

Block Diagram



Pinout



Pin NO.	Pin Name	Function	Pin NO.	Pin Name	Function
1	C_{OMP}	comparator input	5	GND	ground
2	V_{FB}	negative feedback	6	OUTPUT	output
3	I_{SENSE}	current sensitivity	7	V_{CC}	power supply
4	RT/CT	oscillator terminal	8	V_{REF}	referance voltage

Maximum Rated Value (unless otherwise specified, Tamb=25℃)

Parameter	Symbol	Value	Unit
power supply voltage	V_{cc}	30	V
output current	I_o	±1	A
error amplifier current	I_{sink} (EA)	10	mA
error amplifier input voltage	V_{in} (EA)	-0.3 ~ +6.3	V
power consumption	P_D(DIP)	1	W
operating environment temperature	T_{amb}	0 ~ 70	℃
storage temperature	T_{stg}	-55 ~ 150	℃

Electrical Characteristics(unless otherwise specified, V_{cc}=15V, R_T =10kΩ, C_T =3.3nF, T_{amb}=0℃ ~ 70℃)

Parameter	Symbol	Text Condiction	Min	Typ	Max	Unit
Reference power supply section						
reference voltage	V_{REF}	T_j=25C, I_{REF} =1mA	4.9	5	5.1	V
line regulation	ΔV_{REF}	12V≤V_{cc}≤25V		6	20	mV
load regulation	ΔV_{REF}	1mA≤ I_{REF}20mA		6	25	mV
short circuit output current	I_{sc}	T_{amb}=25℃	-30	-100	-180	mA
oscillator section						
oscillation frequency	f_{OSC}	T_j=25℃	47	52	57	kHz
frequency voltage characteristics	Δf/Δ V_{CC}	12V≤V_{cc}≤25V		0.05	1	%
oscillation amplitude	V(OSC)	4 Foot peak value		1.6		Vpp
Error amplifier section (EA)						
input bias current	I_{BIAS}			-0.1	-2	μA
input voltage	V_{in}(EA)	V1 =2.5V	2.42	2.5	2.58	V
open-loop voltage gain	G_{VO}	2V≤VO ≤4V	60	90		dB
current suppression ratio	P_{SRR}	12V≤V_{CC} ≤25V	60	70		dB
output leakage current	I_{SINK}	V_2 =2.7V, V_1 =1.1V	2	6		mA
output sink current	I_{SOURCE}	V_2 =2.3V, V_1 =5V	-0.5	-0.8		mA
high-level output voltage	V_{OH}	V_2 =2.3V，R_L =15kΩ to GND	5	6		V
low-level output voltage	V_{OL}	V_2 =2.7V，R_L =15kΩ to Pin8		0.7	1.1	V

Current sensitivity section						
gain	GV		2.85	3	3.15	V/V
maximum input signal	V_I(MAX)	V_1 =5V	0.9	1	1.1	V
power supply rejection ratio	P_{SRR}	12V≤V_{CC} ≤25V		70		dB
input bias current	I_{BIAS}			-2	-10	μA
Output						
output low level		I_{SINK} =20mA		0.1	0.4	V
output high level	V_{OL}	I_{SINK} =200mA		1.5	2.2	V
rise time		I_{SOURCE} =20mA	13	13.5		V
falling time	V_{OH}	I_{SOURCE} =200mA	12	13		V
output low level	t_r	C_L=1nF		50	150	ns
output high level	t_f	C_L=1nF		50	150	ns
UVL circuits						
starting threshold	V_{TH}(ST)		7.8	8.4	9	V
minimum operating voltage	V_{OPR}(MIN)		7	7.6	8.2	V
PWM						
maximum duty cycle	D (MAX)		94	96		%
minimum duty cycle	D (MIN)				0	%
Current						
starting current	I_{ST}			70	120	uA
action supply current	I_{CC}(OPR)	V_3 =V_2 =0V		11	17	mA
zener voltage	V_Z	I_{cc}=25mA		34		V

Basic Test Circuit