Low Power Polarity-Insensitive RS 485 Transceiver

Description

The SL485N is designed for RS-485/RS-422 communication. It is a full-duplex communication transceiver that includes one driver and one receiver, featuring driver enable (DE) and receiver enable (RE) pins. When disabled, the driver and receiver outputs are in a high-impedance state. It has a fail-safe circuit that ensures the receiver output is correct even if the receiver input is open-circuited or short-circuited. It also has a +15kV ESD (Electrostatic Discharge) protection feature. Additionally, its receiver has a 1/8 unit load input impedance, allowing up to 256 transceivers to be connected on the bus. Compared to traditional 485 chips, the SL485N has an adaptive feature that allows communication regardless of the L1 and L2 connection (no need to distinguish L1 and L2), with a communication rate that must be greater than 25Hz. Its features include:

- ESD protection for L1/L2 pins: +15kV HBM
- Fractional unit load allows up to 256 devices on the bus
- Tri-state R_x and T_x outputs
- Operates on a single +5V power supply
- Package forms: SOP8, DIP8

Applications

- Industrial control
- Electricity meters
- Industrial motor drives
- Automated HVAC systems
- RS485/RS422 interfaces

Functional Description

The SL485N high-speed transceiver for RS-485/RS-422 communication includes one driver and one receiver. It has a fail-safe circuit that ensures the receiver output is a logic high level when the receiver input is open or short-circuited. If all transmitters connected to a terminal-matched bus are disabled (high impedance), the receiver will output a logic high level. The SL485N has a low slew-rate driver that reduces EMI and reflections caused by improper cable termination, achieving error-free data transmission up to 500 kbps. The SL485N is a half-duplex transceiver.

Receiver input filtering

When operating at 500kbps, the SL485N receiver includes input filtering in addition to input hysteresis. This filtering function improves noise suppression for slow-rising and falling differential signals.

Reducing EMI and reflections

The low slew-rate driver of the SL485N reduces EMI and lowers reflections caused by improper terminal matching of the cable.

Bus Attachment 256 Loads

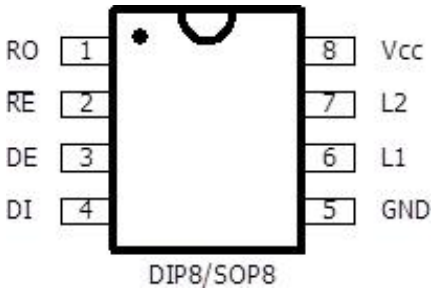
Standard RS-485 receivers have an input impedance of 12KΩ (one unit load), and standard drivers can drive up to 32 unit loads. It has a 1/8 unit load input impedance (greater than 96KΩ), allowing up to 256 transceivers to be connected to the same communication bus. These devices can be combined freely or used in combination with other RS-485 transceivers, as long as the total load on the same bus does not exceed 32 unit loads.

ESD Protection

All pins of the SL485N have ESD discharge protection circuits to prevent damage to the chip from human touch or ESD events during assembly. The driver outputs and receiver inputs have additional enhanced ESD protection circuits, which can withstand ±15kV ESD shocks without damage.

Pin configuration and function

Pin arrangement diagram



Pin function

Pin Number	Pin Name	Function Description
1	RO	Receive Output
2	$\overline{RE}$	Receive Enable: Low level effective, when high, receive output is high impedance.
3	DE	Receive Enable: Low level effective, when high, receive output is high impedance.
4	DI	Transmit Data Input
5	GND	Ground
6	L1	Receive Input/Transmit Output
7	L2	Receive Input/Transmit Output
8	V_{cc}	Power Supply

Electrical Characteristics LimitingParameters(Unlessspecified,T_{amb}=25°C)

Symbol	Parameter	Min	Max	Unit
V_{CC}	Power Supply Voltage	-	+6.0	V
	Control Input Voltage（DE，RE）	-0.5	+6.0	V
	Driver Input Voltage（ DI）	-0.5	+6.0	V
	Driver Output Voltage （L1，L2）	-7.0	+12.0	V
	Receiver Input Voltage （L1，L2）	-7.0	+12.0	V
	Receiver Output Voltage（RO）	-0.3	V_{CC}+0.3	V
T_{STG}	Storage Temperature Range	-65	+160	℃
T_{OP}	Operating Temperature Range	-40	+85	℃
Continuous Power Consumption	8-pin Plastic Encapsulated DIP (Above +70°C)	-	725	mW
	8-pin Plastic Encapsulated SOP (Above +70°C	-	470	mW
	Soldering Temperature (10 seconds)	-	+300	℃

DC Parameters: (Unless specified, V_{CC}=5V±5%, T_{amb} = 25℃)

Parameter		Test Condition		Min	Typ	Max	Unit
Driver Differential Output (No Load)	V_{OD1}	-		-	-	5	V
Driver Differential Output (With Load))	V_{OD2}	Fig 1， R=50Ω **or** R=27Ω		2	3	-	V
Driver Differential Output Voltage Variation (Note 2)	ΔV_{OD}			-	-	0.2	V
Driver Differential Output Voltage Variation (Note 2)	V_{OC}			-	V_{cc} /2	3	V
Driver Common-Mode Output Voltage Variation (Note 2)	ΔV_{OC}			-	-	0.2	V
Input High Voltage	V_{IH}	DE, $\overline{RE}$,DI		2	-	-	V
Input Low Voltage	V_{IL}	DE, $\overline{RE}$,DI		-	-	0.8	V
Input Current	I_{IN1}	DE, $\overline{RE}$,DI		-	-	±2	uA
Input Current (L1,L2) (Note 3)	I_{IN2}	DE=0V, V_{cc}=5V	VI_N=5V	-	40	90	uA
			V_{IN}=0V	-	60	100	
Receiver Differential Input Threshold Voltage	V_{TH}	-7V ≤V_{CM}≤+12V		-100	-	100	mV
Receiver Input Hysteresis	ΔV_{TH}			-	25	-	mV
Receiver Output High Voltage	V_{OH}	I_O=-4mA		VCC-1.5V	-	-	V
Receiver Output Low Voltage	V_{OL}	I_O=4mA		-	-	0.4	V
Receiver End Tri-State (High Impedance) Output Current	I_{OZR}	0.4V ≤V_o≤2.4V		-	±1	-	uA
Receiver Input Impedance	R_{IN}	-7V ≤V_{CM}≤+12V		96	-	-	kΩ
No Load Supply Current	I_{CC}	No load, $\overline{RE}$ =DI=GND or V_{cc}	DE=V_{cc}	-	480	800	uA
			DE=GND	-	450	700	uA
Receiver Output Short Circuit Current	I_{OSR}	0V ≤V_{RO}≤V_{CC}		-	±80	-	mA
ESD Protection		L1 / L2 Between, Human Model		±15	-	-	kV

Note 1: All currents flowing into the device are positive, and currents flowing out of the device are negative; unless otherwise specified, all voltages are referenced to ground. Note 2: ΔVOD and ΔVOC are the respective changes in VOD and VOC when the DI input state changes. Note 3: The diagrams listed are with L1 as port A and L2 as port B, and vice versa.

Switching characteristics: unless otherwise specified, V_{dd} =5V±5%, T_{amb}= 25℃

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Driver Input to Output	t_{DPLH}	Fig3 and Fig 5 RDIFF=50Ω C_{L1}=C_{L2}=100pF	250	-	1000	nS
	t_{DPHL}		250	-	1000	nS
Driver Output Offset | t_{DPLH} – t_{DPHL} |	t_{DSKEW}		-	-3	±100	nS
Driver Rise, Fall Time	t_{DR}		200	-	750	nS
	t_{DF}		200	-	750	nS
Driver Enable to Output High	t_{DZH}	Fig4 and Fig 6, C_L=100pF S2 closed	-	-	2500	nS
Driver Enable to Output Low	t_{DZL}	Fig4 and Fig 6, C_L=100pF S1 closed	-	-	2500	nS
Driver from Low to Off |	t_{DLZ}	Fig 4 and Fig 6, C_L=15pF S1 closed	-	-	100	nS
Driver from High to Off	t_{DHZ}	Fig 4 and Fig 6, C_L=15pF S2 closed	-	-	100	nS
Receiver Input to Output	t_{RPLH}	Fig 7 and Fig 9, | V_{ID} | ≥ 2.0V; V_{ID} rise and fall time	-	-	200	nS
	t_{RPHL}		-	-	200	nS
Differential Receiver Offset |t_{RPLH} - t_{RPHL} |	t_{RSKEW}		-	3	±30	nS
Receiver Enable to Output Low	t_{RZL}	Fig 2 and Fig 8 C_L=100pF S1 closed	-	20	50	nS
Receiver Enable to Output High	t_{RZH}	Fig 2 and Fig 8 C_L=100pF S2 closed	-	20	50	nS
Receiver from Low to Off	t_{RLZ}	Fig= 2 and Fig= 8 C_L=100pF S1 closed	-	20	50	nS
Receiver from High to Off	t_{RHZ}	Fig 2 and Fig 8 C_L=100pF S2 closed	-	20	50	nS
Maximum Data Rate	f_{MAX}		-	500	-	kbps

Polarity characteristics:

The polarity direction of the driver and receiver polarity switches remains consistent. Under the following conditions DE=RE=0V, and RO is low, the polarity direction changes after a period T_s.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Polarity Switch Flip Wait Time	T_s	DE=RE=0, RO is low	45	65	80	ms

Note:

- Test circuit diagrams

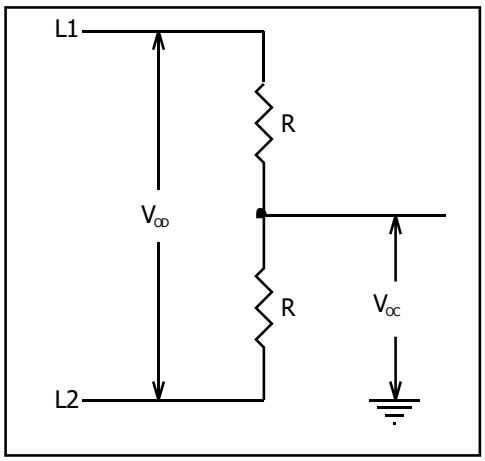


Fig1: driver dc characteristic test load

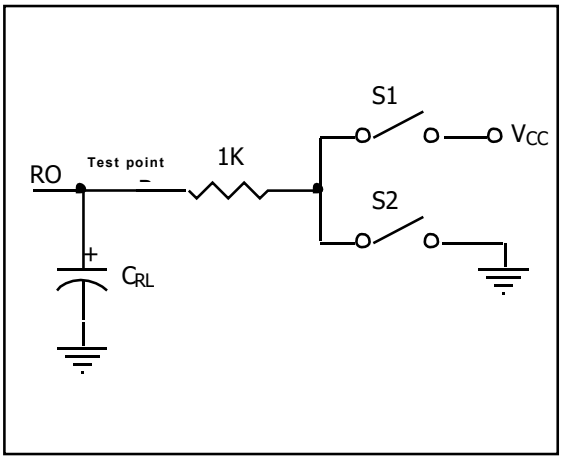


Fig2: receiver enable/shutdown switching characteristic test load

- Test circuit diagrams

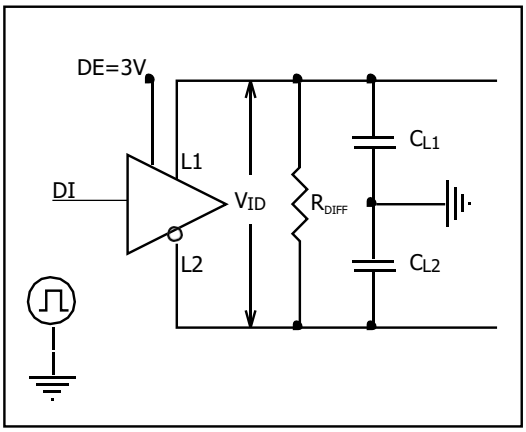


Fig 3: Driver Switching Characteristic Test Load

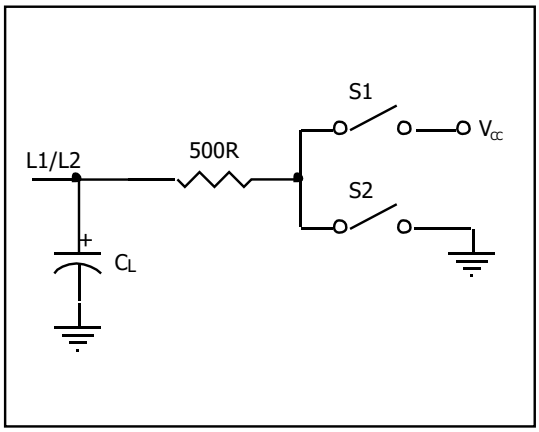


Fig4: Driver Enable/Shutdown Switching Characteristic Test Load

- Test circuit diagram

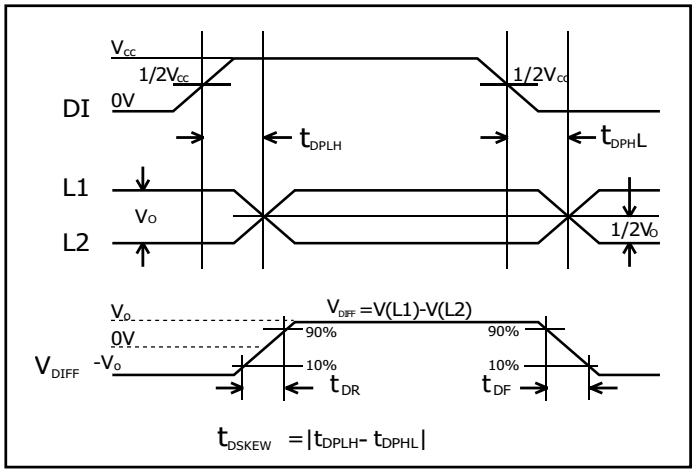


Fig 5: driver transmission delay

- Test circuit diagram

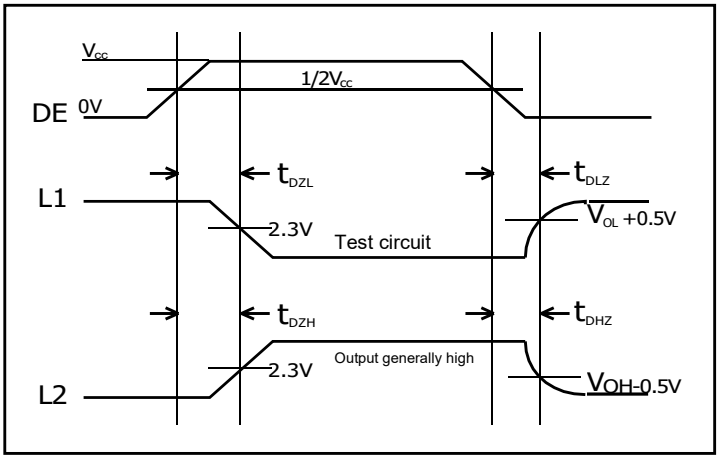


Fig 6: driver enable shutdown timing

- Test circuit diagram

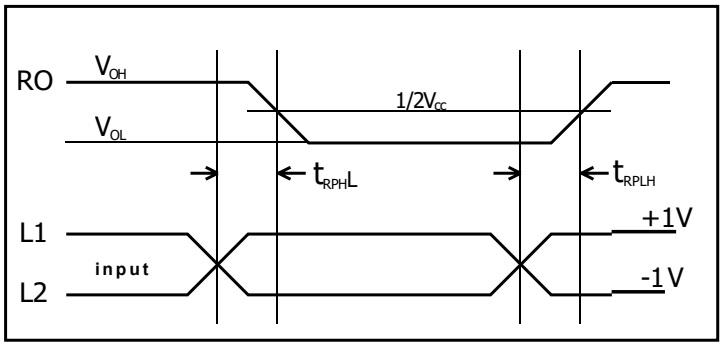


Fig7: Receiver transmission delay timing

- Test circuit diagram

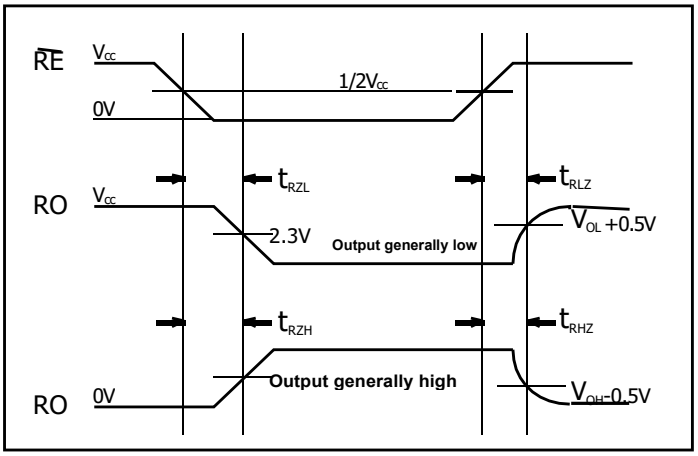


fig 8: receiver enables hut down timing

- Test circuit diagram Figure 9

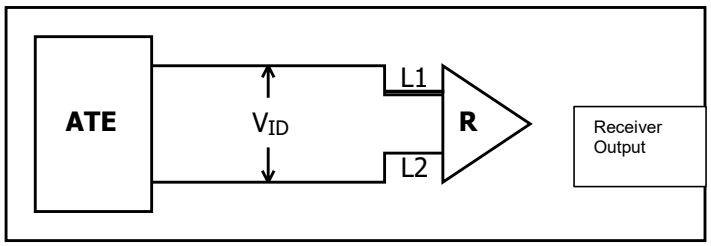
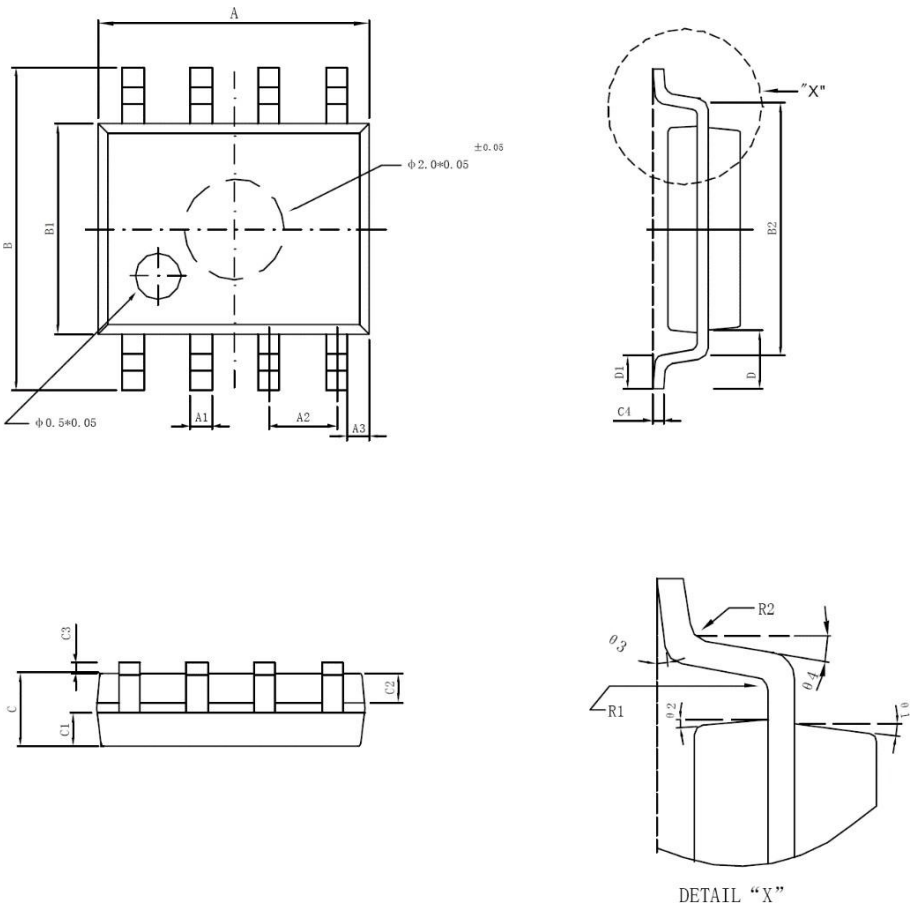


fig9: receiver transmission delay test circuit

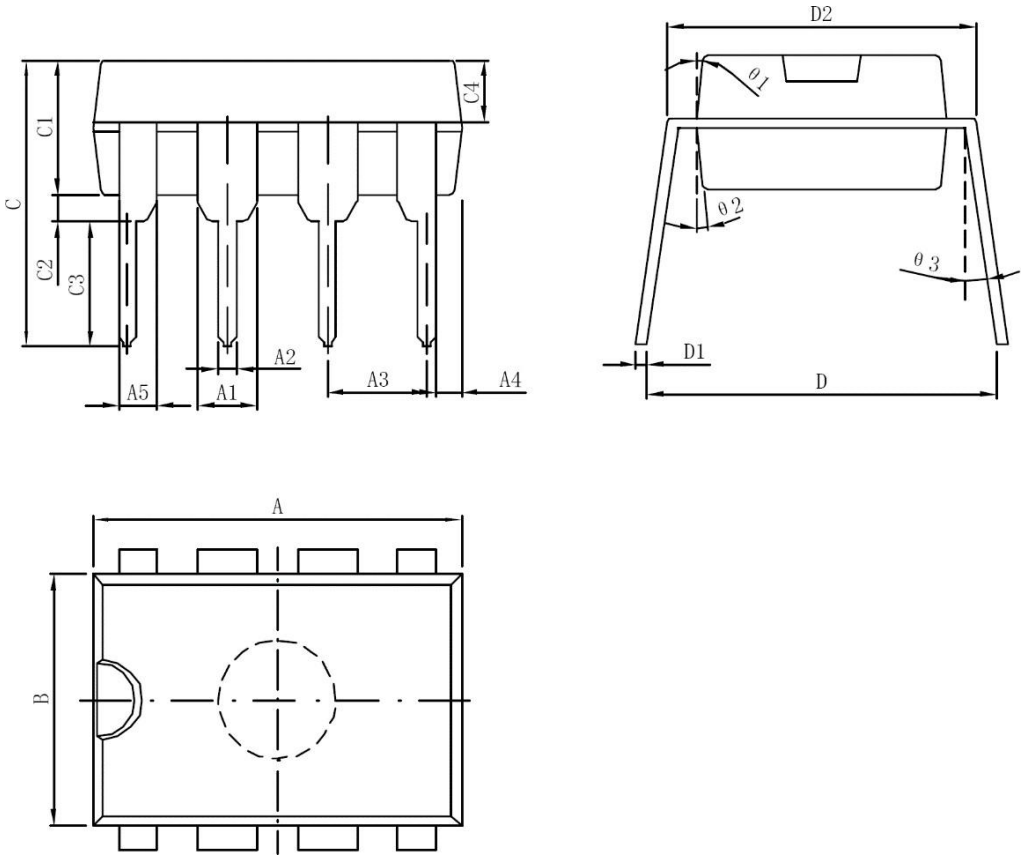
Package dimensions and outline drawing (Unit: mm)

SOP8



Marking	Min (mm)	Max (mm)	Marking	Min (mm)	Max (mm)
A	4.95	5.15	C3	0.10	0.20
A1	0.37	0.47	C4	0.20TYP	
A2	1.27TYP		D	1.05TYP	
A3	0.41TYP		D1	0.50TYP	
B	5.80	6.20	R1	0.07TYP	
B1	3.80	4.00	R2	0.07TYP	
B2	5.0TYP		1	17TYP	
C	1.30	1.50	2	13TYP	
C1	0.55	0.65	3	4TYP	
C2	0.55	0.65	4	12TYP	

DIP8



Marking	Min（mm）	Max（mm）	Marking	Min（mm）	Max（mm）
A	9.30	9.50	C2	0.50	
A1	1.524		C3	3.3	
A2	0.39	0.53	C4	1.57TYP	
A3	2.54		D	8.20	8.80
A4	0.66TYP		D1	0.20	0.35
A5	0.99TYP		D2	7.62	7.87
B	6.3	6.5	1	8 TYP	
C	7.20		2	8 TYP	
C1	3.30	3.50	3	5 TYP	