I²C real-time clock/calendar chip

Features

- Can time seconds, minutes, hours, weekdays, days, months, and years based on a 32.768kHz crystal
- Includes a century flag
- Wide operating voltage range: 1.8 to 5.5V
- Low standby current: typical value of 0.25μA (V_{DD}=3.0V, T_A=25℃)
- I²C bus address: Read, 0A3H; Write, 0A2H
- Programmable clock output frequencies: 32.768kHz, 1024Hz, 32Hz, 1Hz
- Alarm and timer functions
- Power-fail detector
- Internal integrated oscillator capacitor
- Open-drain interrupt pin
- Fully compatible with SL8563x

Applications

- Portable media player
- Mobile phone
- Prepaid electric meter, IC card water meter, IC card gas meter
- Fax machine
- Security electronics

Description

The SL8563x is a low-power CMOS real-time clock/calendar chip that features a programmable clock output, an interrupt output, and a power-fail detector. All addresses and data are serially transmitted via an I²C bus interface. The maximum bus speed is 400Kbits/s, and the embedded byte-addressable register automatically increments after each read or write operation.

Typical application circuit diagram

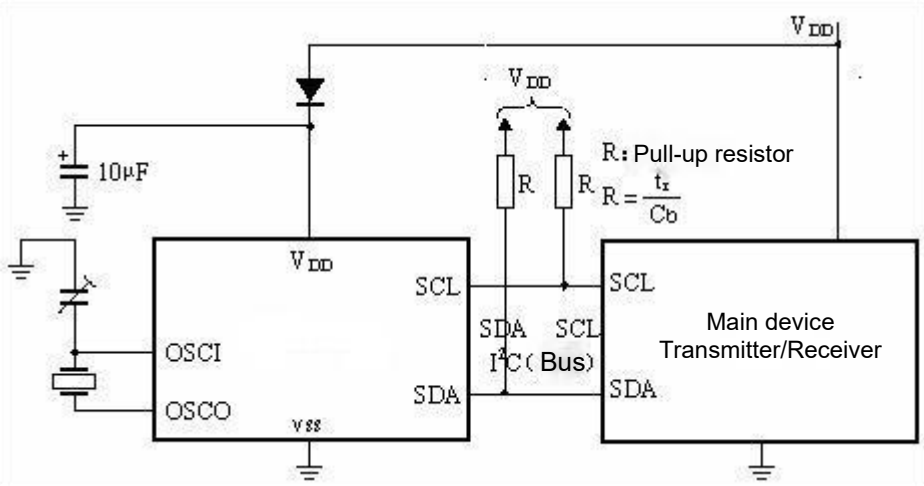


Fig.1 Typical Application Circuit Diagram

Block diagram and pin functions

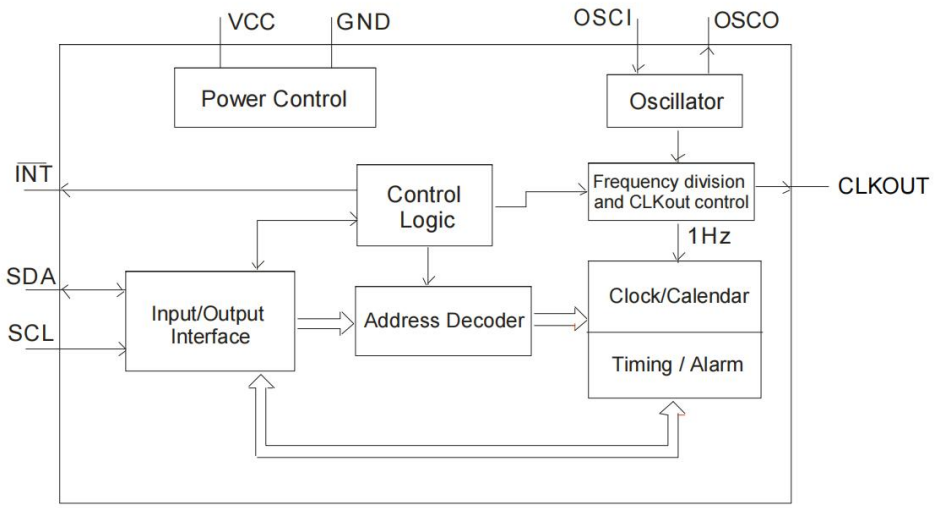


Fig.2 Block Diagram

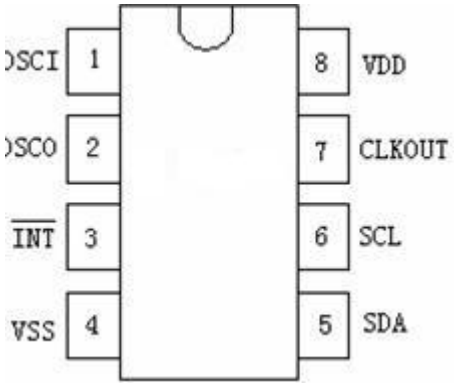


Fig.3 Pinout

Pin Description

Pin Number	Symbol	Description	Pin Number	Symbol	Description
1	OSCI	oscillator input	5	SDA	serial data I/O
2	OSCO	oscillator output	6	SCL	serial clock input
3	INT	interrupt output (open drain)	7	CLKOUT	clock output (open drain)
4	V_{SS}	ground	8	V_{DD}	positive power supply

Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage	V_{DD}	-0.5	+6.5	W
Power supply current	I_{DD}	-50	+50	mA
Input voltage for SCL and SDA pins	V_I	-0.5	+6.5	V
Input voltage for OSCI pin		-0.5	V_{DD}+0.5	V
Output voltage for CLKOUT and INT pins	V_O	-0.5	+6.5	V
DC input current for all input ports	I_I	-10	+10	mA
DC output current for all output ports	I_O	-10	+10	mA
Total power dissipation	P		300	mW
Operating temperature	T_A	-40	+85	℃
Storage temperature	T_S	-65	+150	℃

Electrical characteristics parameters

DC electrical characteristics

(unless otherwise specified, Vn=1.8~5.5V, Vs=0V, Ta=-40~+85℃, fe=32.768kHz, quartz crystal Rs=40kΩ, CL=BpF).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply						
operating voltage	V_{DD}	I^2C bus failure,T_A=25℃[1]	1	-	5.5	V
		I^2C bus valid,f=400kHZ[1]	1.8	-	5.5	V
operating voltage to provide reliable clock/calendar data		T_A=25℃	V_{LOW}	-	5.5	V
working current 1	I_{DD1}	f_{SCL}=400kHz	-	-	800	-
CLKOUT is valid (FE=1)		f_{SCL}=100kHz	-	-	200	-
working current 2 CLKOUT stop (FE=0)	I_{DD2}	f_{SCL};=0Hz,T_A=25℃				
		V_{DD}=5.0V	-	275	550	nA
		V_{DD}=3.0W	-	250	500	nA
		V_{DD}=2.0V	-	225	450	nA
		f_{SCL}=0Hz,T_A=-40~+85℃				
		V_{DD}=5.0V	-	500	750	nA
		V_{DD}=3.0V	-	400	650	nA
		V_{DD}=2.0V	-	400	600	nA
working current 3CLKOUT=32.768kHz	I_{DD3}	f_{SCL}=0Hz,T_A=25℃				
		V_{DD}=5.0V	-	825	600	nA
		V_{DD}=3.0V	-	550	1000	nA
		V_{DD}=2.0V	-	425	800	nA
		f_{SCL}=0Hz,T_A=-40~+85℃				
		V_{DD}=5.0V	-	950	1700	nA
		V_{DD}=3.0V	-	650	1100	nA
		V_{DD}=2.0V	-	500	900	nA
Input						
low level input voltage	V_{IL}		V_{SS}	-	0.3V_{DD}	V
high level input voltage	V_{IH}		0.7V_{DD}	-	V_{DD}	V
input leakage current	I_{LI}	V=V_{DD} or V_{SS}	-1	0	1	μA
input capacitance	C_I	[3]	-	-	7	pF
Output						
SDA low level output current	I_{OLS}	V_{CE}=0.4V,V_{DD}=5.0V	-3	-	-	mA
INT low level output current	I_{OLI}	V_{CE}=0.4V,V_{DD}=5.0V	-1	-	-	mA
CLKOUT low level output current	I_{OLC}	V_{CE}=0.4V,V_{DD}=5.0V	-1	-	-	mA
CLKOUT high level output current	I_{OHC}	V_{CE}=4.6V,V_{DD}=5.0V	1	-	-	mA
output leakage current	I_{Lo}	V0=V_{DD} or V_{SS}	-1	0	1	μA
Voltage detector						
power-off detection voltage	V_{LOW}	Ta=25℃	-	0.9	1	V

1. Oscillator reliably starts upon power-up: VDD (minimum, power-up) = VDD (minimum) + 0.3V.
2. Timer source clock = 1/60Hz; both SCL and SDA are at VDD.
3. Tested based on samples.

AC characteristics (unless otherwise specified, V_{DD} = 1.8~5.5V, V_{SS} = 0V; T_A = -40 to +85℃; f_{OSC} = 32.768KHz; quartz crystal Rs = 40kΩ, C_L = 8pF).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillator						
precision load capacitance	C_{INT}		15	25	35	pF
oscillator stability	$\triangle f_{osc}/f_{osc}$	$\triangle V_{DD}$=200mV,Ta=25℃	—	2×10^{-7}	—	—
Quartz crystal parameters(f=32.768kHz)						
shenlian resistors	R_S		—	—	40	kQ
parallel loadcapacitance	C_L		—	10	—	pF
trimmer capacitor	C_I		5	—	25	pF
CLKOUT Output						
CLKOUT duty cycle	δ_{CLKOUT}	[1]	—	50	—	%
I2C Bus Timing Characteristics						
SCL clock cycle	f_{scL}	[4]	—	—	400	kHz
starting condition holding time	t_{HDSTA}		0.6	—	—	μs
repeated start condition setup time	t_{SUSTA}		0.6	—	—	μs
SCL low level time	t_{Low}		1.3	—	—	μs
SCL high time	t_{HIGH}		0.6	—	—	μs
rising edge time of SCL and SDA	t_r		—	—	0.3	μs
falling edge time of SCL and SDA	t_r		—	—	0.3	μs
bus load capacitance	C_b		—	—	400	pF
data setup time	t_{SUDAY}		100	—	—	ns
data hold time	t_{HDDAY}		0	—		ns
stop condition setup time	t_{SUSTO}		0.6	—	—	μs
acceptable bus spike width	t_{SW}		—	—	50	ns

1. Unless otherwise specified, f_{CLKOUT} = 32.768kHz.
2. All timing values are valid within the operating voltage range (T_A condition). Refer to input voltage variations between V_{SS} and V_{DD} for V_{IL} and V_{IH} values.
3. Access time for I^2C bus between two starts and one stop condition must be less than 1s.

I²C bus timing waveform

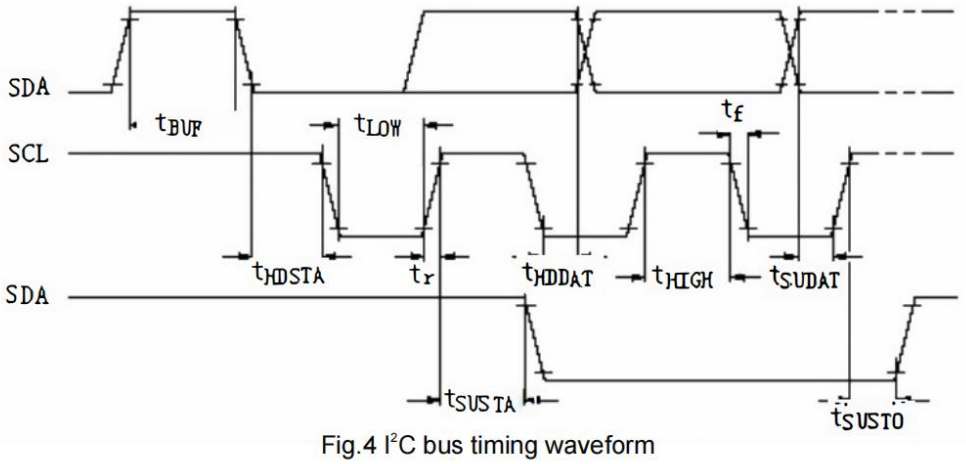
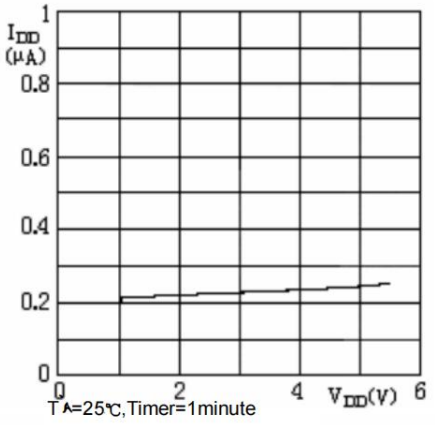
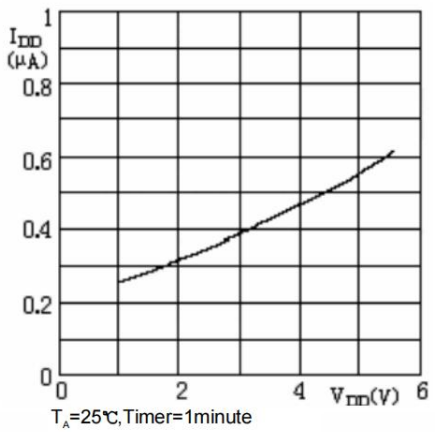


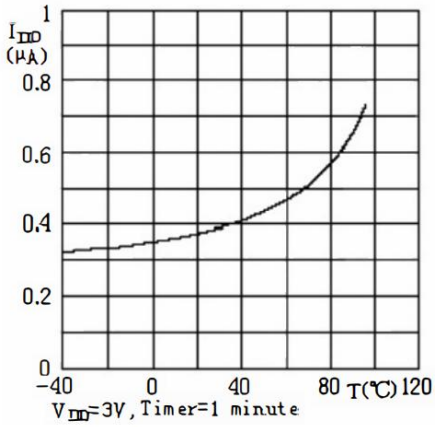
Fig.4 I²C bus timing waveform



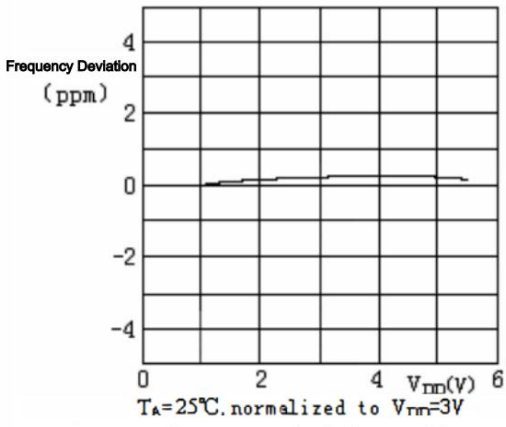
I_{DD} vs. V_{DD} when CLKOUT is disabled



CLKOUT=32.768KHz, I_{DD} vs. V_{DD}



CLKOUT=32.768kHz, I_{DD} vs T_A



Frequency deviation vs. V_{DD}

Description

The SL8563x features 16 8-bit registers, an auto-incrementing address register, a built-in 32.768kHz oscillator with an integrated capacitor, a prescaler for providing clock source to the real-time clock (RTC), a programmable clock output, a timer, an alarm, a brown-out detector, and a 400kHz I^2C bus interface.

All 16 registers are designed as addressable 8-bit parallel registers, though not all bits are utilized. The first two registers (internal addresses 00H and 01H) serve as control and status registers. Addresses 02H to 08H are used for the clock counters (seconds through year counters), while addresses 09H to 0CH are allocated for alarm registers (defining alarm conditions). Address 0DH controls the output frequency of the CLKOUT pin, and addresses 0EH and 0FH are designated for the timer control and timer registers, respectively. The seconds, minutes, hours, day, month, year, minute alarm, hour alarm registers use BCD encoding format, while the weekday and weekday alarm registers do not use BCD encoding.

Alarm function mode

When one or more alarm register MSBs (AE = Alarm Enable) are cleared to 0, the corresponding alarm condition is valid, so that an alarm will be generated once every minute to once a week. Set the alarm flag bit AF (bit 3 of control/status register 2) to generate an interrupt. AF can only be cleared by software.

Timer

The 8-bit countdown timer (address 0FH) is controlled by the timer control register (address 0EH, refer to Table 22). This register configures the timer's frequency (4096Hz, 64Hz, 1Hz, or 1/60Hz) and enables or disables the timer. The timer counts down an 8-bit binary number set by software. At the end of each countdown, the timer sets the TF flag (see Table 4), which triggers an interrupt (INT). Each countdown cycle generates a pulse as the interrupt signal. The TF timer flag can only be cleared through software. TI/TP (see Table 4) controls the conditions for interrupt generation. When reading the timer, it returns the current countdown value.

CLKOUT Output

The pin CLKOUT can output a programmable square wave. The CLKOUT frequency register (address 0DH, see Table 20) determines the frequency of the output square wave, which can be 32.768kHz (default), 1024Hz, 32Hz, or 1Hz. CLKOUT is an open-drain output pin that is active when powered and becomes high impedance when inactive.

Reset

SL8563x has a built-in reset circuit, which starts to work when the oscillator stops working. In the reset state, the I^2C bus is initialized, and all registers (including address pointer) will be cleared except TF, VL, TD1, TD0, TESTC, and AE bits are set to logic 1.

Brownout detection and clock monitoring

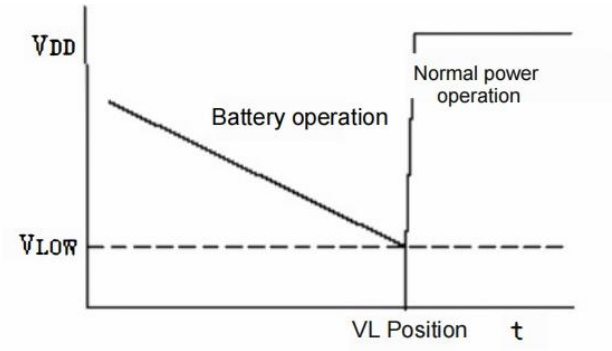


Figure 8. Power-Off Detection

The SL8563x integrates a brown-out detection circuit, where the VL bit (Voltage Low, bit 7 of the seconds register) is set to 1 when V_{DD} drops below V_{LOW}. This indicates potential inaccuracies in clock/calendar data. The VL flag can only be cleared via software. When V_{DD} slowly decreases (e.g., due to battery power) to V_{LOW}, VL is set, indicating a potential interrupt condition.

Register structure

Table 1. Register Overview

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00H	control/status register 1	TEST	0	STOP	0	TESTC	0	0	0
01H	control/status register 2	0	0	0	TI/TP	AF	TF	AIE	TIE
0DH	CLKOUT frequency register	FE	—	—	—	—	—	FD1	FD0
0EH	timer control register	TE	—	—	—	—	—	TD1	TD0
0FH	timer countdown register	timer countdown value							

Bits marked with “—” are invalid, and bits marked with “0” should be set to logic 0.

Table 2. BCD Format Register Overview

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02H	seconds	VL	00～59BCD code format number						
03H	minutes	—	00～59BCD code format number						
04H	hours	—	—	00～23BCD code format number					
05H	day	—	—	01～31BCD code format number					
06H	weekday	—	—	—	—	—	0～6		
07H	monthcentury	C	—	—	01～12BCD code format number				
08H	year	00～99BCD code format number							
09H	minute alarm	AE	00～59BCD code format number						
0AH	hour alarm	AE	—	00～23BCD code format number					
0BH	day alarm	AE	—	01～31BCD code format number					
0CH	weekday alarm	AE	—	—	—	—	0～6		

The position marked with "—" is invalid.

Control/Status Register 1

Table 3.Control/Status Register 1 (Address 00H)Bit Description

Position No.	Symbol	Description
7	TEST1	TEST1=0:Normal mode TEST1=1:EXT_CLK Test Mode
5	STOP	STOP=0:RTCClock running;STOP=1:All RTC dividers are asynchronously set to logic 0, and the RTC clock stops running. (CLKOUT is still available at 32.768kHz)
3	TESTC	TESTC=0:Power reset function disabled (set to logic O in normal mode) TESTC=1:Power reset function is effective
6,4,2~0		The default value is logic 0.

Control/Status Register 2

TF and AF bits:When an alarm occurs,AF is set to logic 1.Similarly,when the countdown of a timer reaches zero,TF is set to logic 1.Both bits can only be modified through software.If both timer and alarm interrupts are needed in an application,reading these two bytes can identify the interrupt source.To clear a bit within a write cycle and prevent flag rewriting,a logical AND operation should be performed.

TIE and AIE bits:These two bits are used to enable interrupt generation.When both AIE and TIE are set,interrupts are generated as a logical OR of these two bits.

Table 4.Bit Description of Control/Status Register 2(Address 01h)

Position No.	Symbol	Description
7,6,5		The default value is logic 0.
4	TI/TP	TI/TP=0:When TF is valid,INT is valid (depending on the state of TIE) TI/TP=1:INT,pulse valid,see Table 5(depends on the state of TIE) Note:IfAF and AIE are both valid,INTis always valid
3	AF	AF=0:During read operation,the alam flag is invalid;during write operation,the alarm flag is cleared;AF=1:During read operation,the alarm flag is valid;during write operation,the alarm flag remains unchanged.
2	TF	TF=0:When reading,the timer flag is invalid;when writing,the timer flag is cleared; TF=1:When reading,the timer flag is valid;when writing,the timer flag remains unchanged
1	AIE	AIE=0:Alarm interrupt is disabled AIE=1:alarm interrupt is enabled
0	TIE	TIE=0:Timer interrupt is disabled TIE=1:Timer interrupt is enabled

Table 5.INT Operation(Bit TI/TP=1)

Clock Source(Hz)	~INTcycle[1]	
	n=1[2]	n>1
4096	1/8192	1/4096
64	1/128	1/64
1	1/64	1/64
1/60	1/64	1/64

[1].TF and INT are both valid;
[2].n is the value of the countdown timer.When n=0,the timer stops working.

Seconds, minutes, and hours registers

Table 6. Seconds/VL Register (Address 02H) Bit Description

Position No.	Symbol	Description
6～0	(Second)	Represents the current second value in BCD format, ranging from 00 to 99. For example, 1011001 represents 59 seconds.
7	VL	VL=0：Ensure accurate clock/calendar data,VL=1：Accurate clock/calendar data is not guaranteed

Table 7. Minute Register (Address 03H) Bit Description

Position No.	Symbol	Description
7	—	invalid
6～0	(minute)	Represents the current minute value in BCD format, ranging from 00 to 59

Table 8. Hour Register (Address 04H) Bit Description

Position No.	Symbol	Description
7，6	—	invalid
5～0	(Hour)	Represents the current hour value in BCD format, ranging from 00 to 23

Day, weekday, month/century, and year registers

Table 9. Day Register (Address 05H) Bit Description

Position No.	Symbol	Description
7，6	—	invalid
5～0	(day)	Represents the current day value in BCD format, ranging from 01 to 31. If the current year counter value is a leap year, 8563 automatically adds a value to February to make it 29 days.

Table 10. Weekday Register (Address 06H) Bit Description

Position No.	Symbol	Description
7～3	—	invalid
2～0	(Week)	Represents the current week value, ranging from 0 to 6. See Table 11. These bits can also be reallocated by the user.

Table 11. Weekly Distribution Table

Day	Bit 2	Bit 1	Bit 0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

Table 12. Month/Century Register (Address 07H) Bit Description

Position No.	Symbol	Description
7	C	Century bit: C=0 specifies the century as 20XX; C=1 specifies the century as 19XX, where “XX” is the value in the year register, see Table 14. When the year changes from 99 to 00, the century bit will change.
6，5	—	invalid
4～0	(Month)	Represents the current month value in BCD format, ranging from 01 to 12, see Table 13

Table 13. Monthly Allocation Table

The months	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

Table 14. Year Register (Address 08H) Bit Description

Position No.	Symbol	Description
7～0	(year)	Represents the current year value in BCD format, ranging from 00 to 99

Alarm Control Register

When one or more alarm registers are written with valid minute, hour, day, or weekday values, and their corresponding AE (Alarm Enable) bits are logic 0, and these values match the current minute, hour, day, or weekday values, the AF (Alarm Flag) is set. AF retains this set state until cleared by software. Once cleared, AF can only be set again when the time increments and matches the alarm conditions once more. Alarm registers are ignored when their respective AE bits are set to logic 1.

Table 15. Minute Alarm Register (Address 09H) Bit Description

Position No.	Symbol	Description
7	AE	AE=0，Minute alarm effective；AE=1，Minute alarm invalid
6～0	Minute alarm	Represents the minute alarm value in BCD format, the value is 00～59

Table 16. Hour Alarm Register (Address 0AH) Bit Description

Position No.	Symbol	Description
7	AE	AE=0，Hour alarm effective；AE=1，Hour alarm invalid
5～0	Hour alarm	Represents the hour alarm value in BCD format, the value is 00~23

Table 17. Daily Alarm Register (Address 0BH) Bit Description

Position No.	Symbol	Description
7	AE	AE=0，Daily alarm is effective；AE=1，Day alarm invalid
5～0	Daily alarm	Represents the daily alarm value in BCD format, with a value of 01 to 31

Table 18. Week Alarm Register (Address 0CH) Bit Description

Position No.	Symbol	Description
7	AE	AE=0，Weekly alarm valid；AE=1，Week alarm invalid
2～0	Weekly alarm	Represents the weekday alarm value in BCD format, the value is 0 to 6

CLKOUT Frequency Register

Table 19. CLKOUT Frequency Register (Address 0Dh) Bit Description

Position No.	Symbol	Description
7	FE	FE=0：CLKOUT outputs are disabled and set to high impedance FE=1：CLKOUT output valid
6～2	—	invalid
1	FD1	The frequency output pin (f_{CLKOUT}) used to control CLKOUT is shown in Table 20.
0	FD0	The frequency output pin (f_{CLKOUT}) used to control CLKOUT is shown in Table 20.

Table 20. CLKOUT Frequency Selection Table

FD1	FD0	f_{CLKOUT}
0	0	32.768kHz
0	1	1024Hz
1	0	32Hz
1	1	1Hz

Countdown Timer Register

The timer register is an 8-bit byte countdown timer, its validity determined by bit TE in the timer controller. The timer clock can also be selected via the timer controller. Other timer functions, such as interrupt generation, are controlled by Control/Status Register 2. To accurately read back the countdown value, the I^2C bus clock SCL should be at least twice the frequency of the selected timer clock.

Table 21. Timer Control Register (Address 0EH) Bit Description

Position No.	Symbol	Description
7	TE	TE=0：Timer invalid； TE=1：Timer is valid.
6～2	—	useless
1	TD1	The timer clock frequency selection bits determine the clock frequency of the countdown timer, as specified in Table 22. When not in use, TD1 and TD0 should be set to "11" (1/60Hz) to minimize power consumption.
0		

Table 22. Timer Clock Frequency Selection

TD1	TD0	Timer Clock Frequency(Hz)
0	0	4096
0	1	64
1	0	1
1	1	1/60

Table 23. Timer Countdown Value Register (Address 0FH) Bit Description

Position No.	Symbol	Description
7～0	timer countdown value	Countdown value "n", countdown period = n/clock frequency.

EXT_CLK Test Mode

The test mode is used for online testing, establishing test patterns, and controlling RTC operations. The test mode is initiated by setting bit TEST1 of Control/Status Register 1, where the CLKOUT pin becomes an input. In test mode, a frequency signal input through the CLKOUT pin replaces the internal 64Hz signal, with each 64 rising edges generating a 1-second time increment.

Note: When entering EXT_CLK test mode, the clock is not synchronized with the internal 64Hz clock, and the prescaling state cannot be determined.

Operation examples

1. Enter EXT_CLK test mode by setting bit 7 of Control/Status Register 1 (TEST=1).
2. Set bit 5 of Control/Status Register 1 (STOP=1).
3. Clear bit 5 of Control/Status Register 1 (STOP=0).
4. Set the Time Register (seconds, minutes, hours, day, weekday, month/century, and year) to the desired values.
5. Provide 32 clock pulses to CLKOUT.
6. Read the Time Register and observe the first change.
7. Provide 64 clock pulses to CLKOUT.
8. Read the Time Register and observe the second change. If additional increments of the Time Register are required, repeat steps 7 and 8.

Power-On-Reset (POR) Failure Mode

The duration of POR (Power-On Reset) is directly related to the start-up time of the oscillator. An embedded circuit with an extended start-up time can disable POR, accelerating device testing. The signal waveforms for I^2C bus pins SDA and SCL must adhere to the timings shown in Figure 9, where all timings represent minimum required values.

Upon entering the disabled mode, the chip immediately halts reset and transitions to EXT_CLK test mode via the I^2C bus. Clearing the TESTC bit (logic 0) eliminates the disabled mode, allowing re-entry into disabled mode only after setting TESTC to logic 1. Setting TESTC to logic 0 during normal operation is meaningless unless preventing entry into POR disabled mode is desired.

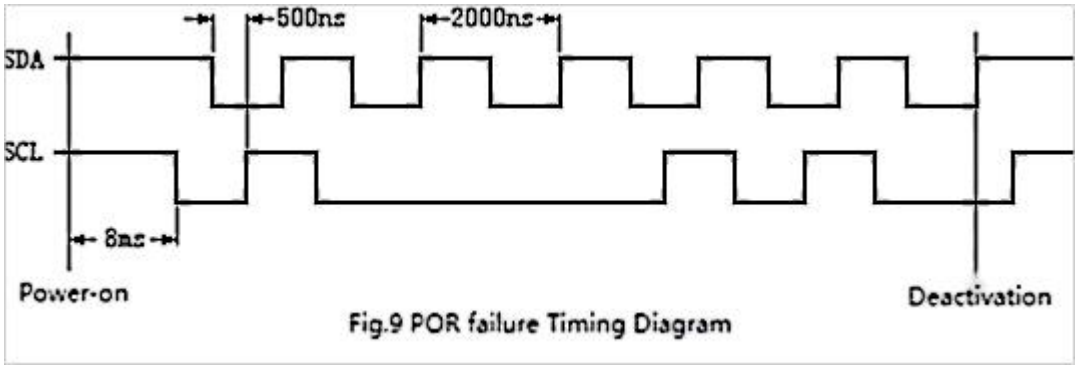


Fig.9 POR failure Timing Diagram

Serial interface

The SL8563x uses a serial I²C bus interface.

I²C Bus characteristics

The I²C bus communicates information between different chips and modules using two lines: SDA for serial data and SCL for serial clock. Both lines must be connected to a positive power source through a pull-up resistor. Data transmission occurs only when the bus is idle.

As depicted in Figure 10, the transmitting device generates information, the receiving device accepts it, the controlling device is the master, and the controlled device is the slave.

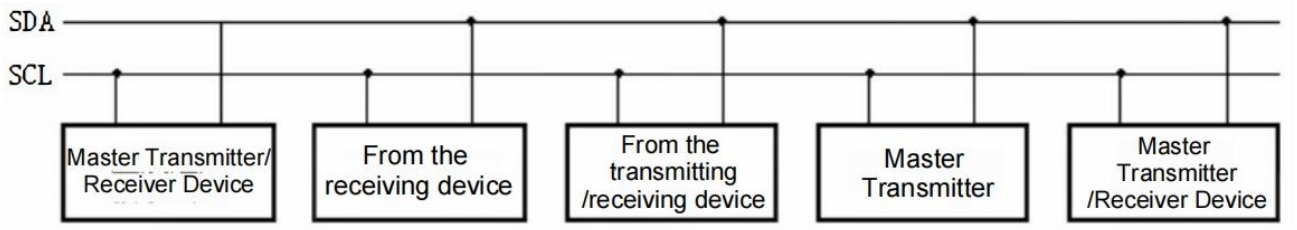


Fig.10 I²C Bus System Configuration Diagram

Start (START) and stop (STOP) conditions

When the bus is idle, both the data line and the clock line maintain a high level. The start condition (S) occurs when the data line transitions from high to low during a high clock pulse. The stop condition (P) occurs when the data line transitions from low to high during a high clock pulse, as shown in Figure 11.

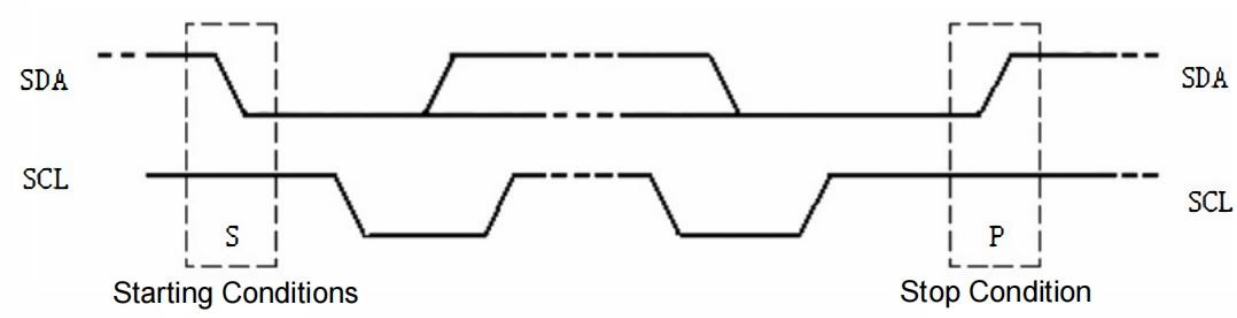


Fig.11 I²C Bus Start (Start) And Stop (Stop) Condition Definition

Bit transfer

Each clock pulse transmits one data bit, and the data on the SDA line should remain stable during the high phase of the clock pulse. Otherwise, the data on the SDA line could inadvertently become control signals, as referenced in Figure 12.

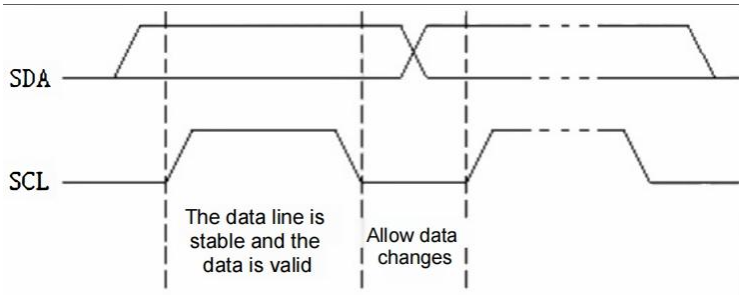


Fig.12 Bit Transfer on the I²C Bus

Acknowledge bit

There is no limit to the number of data bytes a transmitter can send to a receiver between the start and stop conditions. After each 8-bit byte, an acknowledgment (ACK) bit is appended. The transmitter generates a high-level ACK bit, prompting the master device to produce an additional ACK clock pulse. The receiver must generate an ACK bit after receiving each byte, and the master receiver must also produce an ACK bit after receiving each byte transmitted by the transmitter. When the ACK clock pulse appears, the SDA line should remain at a low level (considering setup and hold times). The transmitter should transition to a low level when the last byte is received from the device, causing the receiver to generate an ACK bit, allowing the master device to generate a stop condition.

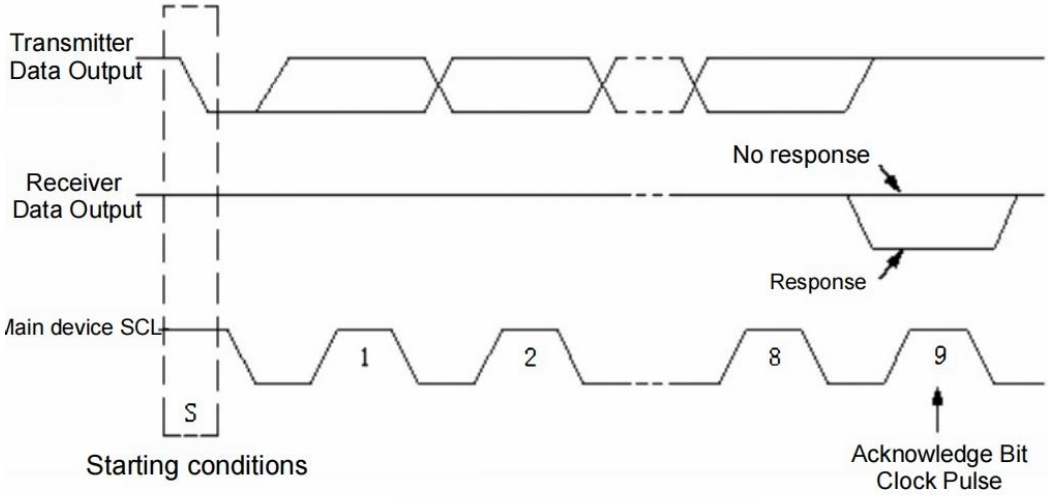


Fig.13 I²C Bus Acknowledge Bit

I²C Bus protocol

Note: Before transmitting data over the I²C bus, the receiving device must first acknowledge its address. Upon initiation of the I²C bus, this address is transmitted along with the first byte of data. The SL8563x can function as either a slave receiver or transmitter. In this mode, the clock signal line SCL functions strictly as an input signal line, while the data signal line SDA serves as a bidirectional signal line.

The slave address for the SL8563x is detailed in Figure 14.

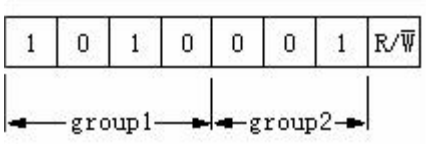


Fig.14 Slave Address

Clock/calendar read/write cycles

The serial I²C bus of SL8563x has three configuration options for read/write cycles, as depicted in Figures 15, 16, and 17. The address in these figures is a 4-bit number used to indicate the next register to access, with the upper four bits of the address being unused.

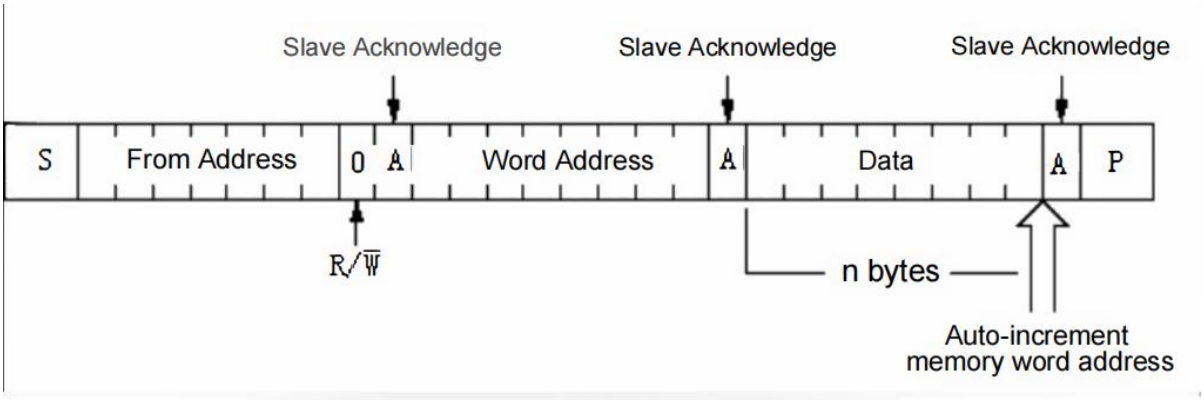


Fig.15 Master Transmitter To Slave Receiver (Write Mode)

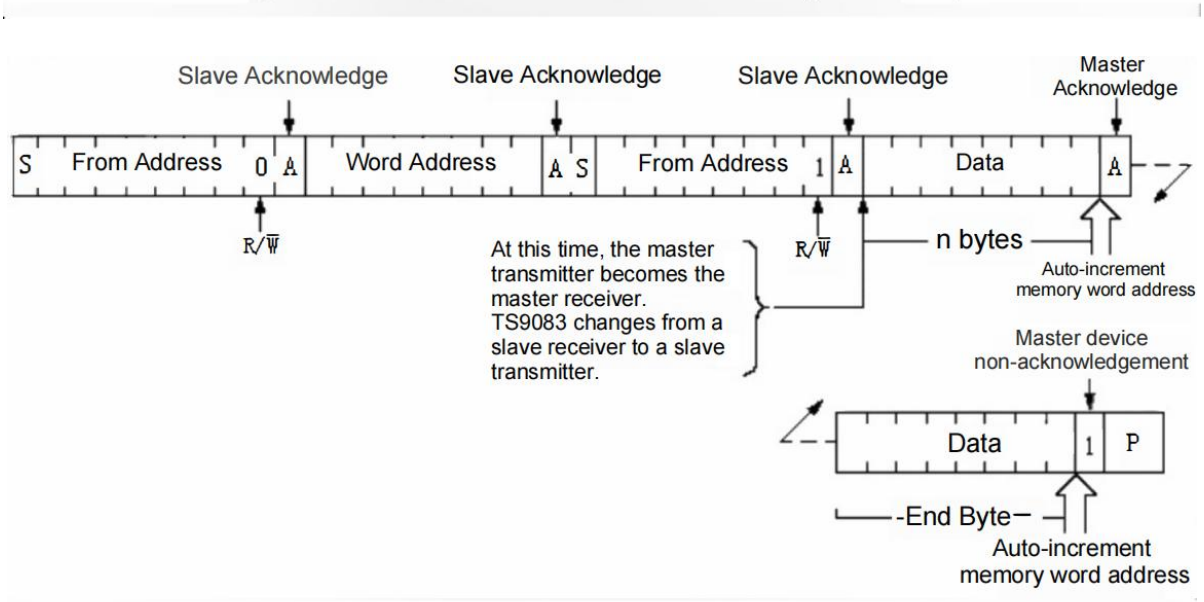


Fig.16 Master Reads Data After Setting Word Address (Write Address, Read Data)

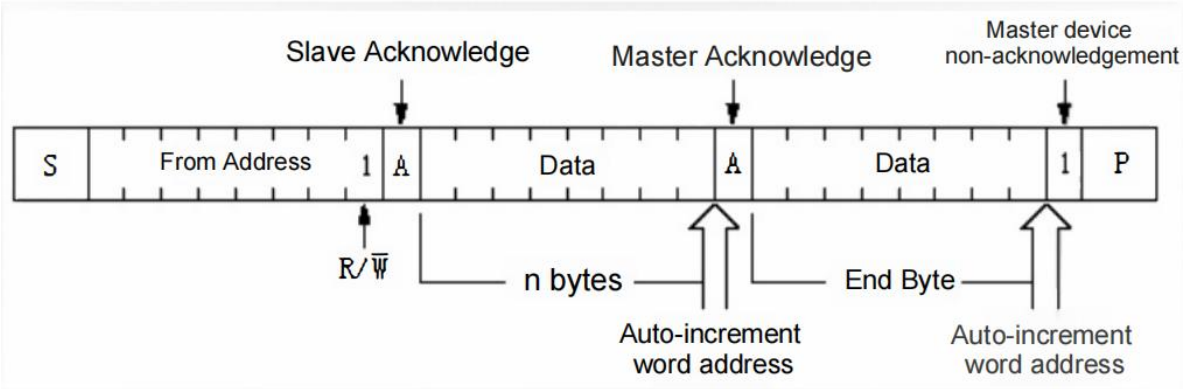


Fig.17 Master Reads Data After The First Byte Of Data From The Slave (Read Mode)

Quartz crystal frequency adjustment

Method 1: Fixed OSCI Capacitor — Calculate the required average capacitance. Use this fixed capacitor value; upon powering, the frequency measured at the CLKOUT pin should be 32.768kHz. Deviation in the measured frequency depends on the quartz crystal, capacitor tolerance, and device variation (typically $\pm 5\times10^{-6}$). Average deviation can be controlled within ± 5 minutes per year.

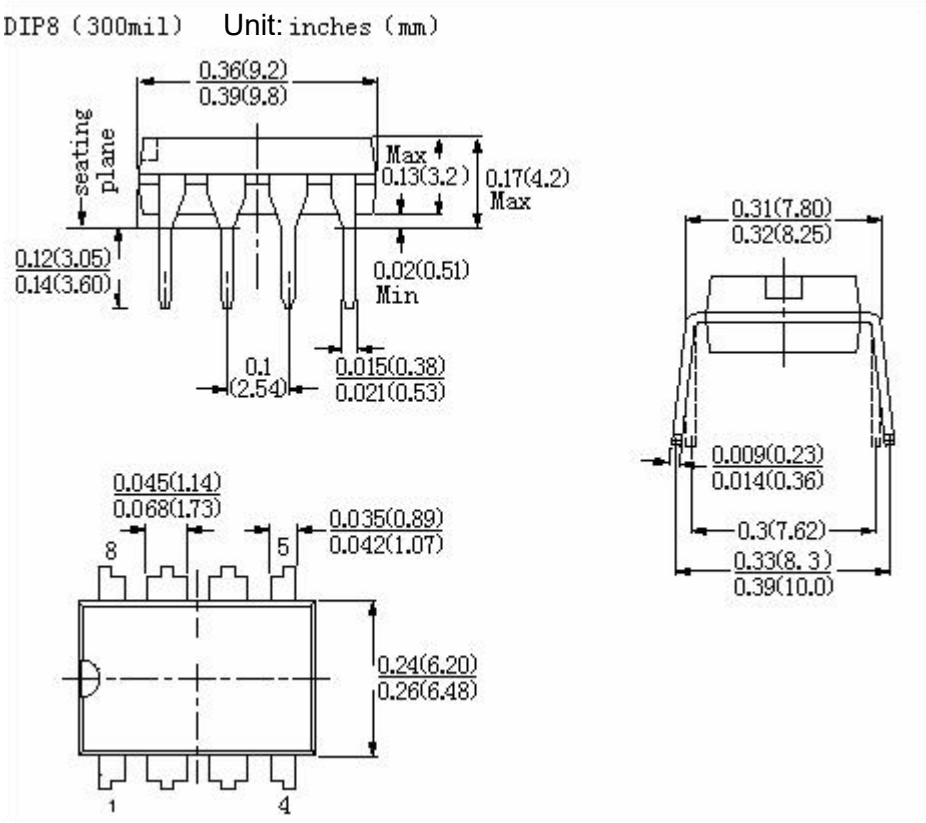
Method 2: OSCI Fine Tuning Capacitor — Achieve the precise oscillator frequency by adjusting the fine tuning capacitor on the OSCI pin. Upon powering, the frequency at the CLKOUT pin can be measured to be 32.768kHz.

Method 3: OSCO Output — Directly measure the output at OSCO (considering the capacitance of the test probe).

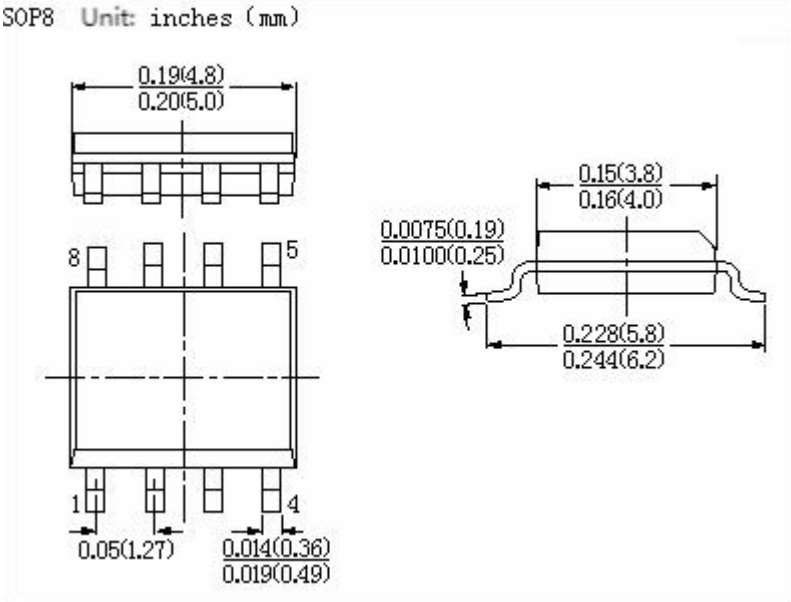
Ordering information

Model	Temperature Range	Package
SL8563D	-40～+85℃	DIP8
SL8563T		SOP8
SL8563S		MSOP8

Package dimensions



SOP8 Unit: inches (mm)



MSOP8 Unit: inches (mm)