12-bit high-resolution high-speed 3.3V-5.25V operating voltage 200-500KSPS analog-to-digital converter (ADC)

Description

SL101S021 is a 12-bit ADC (Analog-to-Digital Converter) chip with the basic characteristics of high resolution, low power consumption, small size and unipolarity. The performance parameters of SL101S021 cover a wide sampling range of 50KSPS to 200KSPS, and are not only valid at a specific sampling rate. The converter is based on a successive approximation register architecture with an internal sample-and-hold circuit. SL101S021 is powered by a single power supply of 3.3 V to 5.25 V and has a power saving mode.

The SL101S021 is available in a 6-pin SOT-23 package and operates over the -40°C to 85°C temperature range.

Features

Sampling rate: 50 – 200 KSPS

10-bit resolution

Supply voltage range: 3.3V to 5.25V

Low power consumption (typical)

2.30mW   5V   200 KSPS   1.10mW   3.3V   200 KSPS

Maximum error ±1LSB INL   ±1LSB DNL

0—VA uni-polar single channel input

SPI, QSPI™, MICROWIRE™, DSP serial interface

6 pin SOT-23 package

Application

Portable systems

Remote data collection

Instrumentation and control systems

Optical sensors

Battery powered system
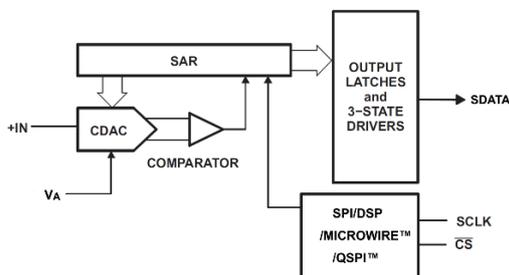
Schematic

Packaging effect diagram

Pin-compatible resolution and speed alternative

| Resolution	Specify the sampling rate range			
	50 to 200 KSPS	200 to 500 KSPS	500 to 800 KSPS	800 to 1000 KSPS
12-bit	SL121S021	SL121S051	SL121S101	SL121S101E
10-bit	SL101S021	SL101S051	SL101S101	SL101S101E
8-bit	SL081S021	SL081S051	SL081S101	SL081S101E

1.Main technical parameters

3.3 V - 5.25 V single power supply
12-bit resolution, no missing codes
Differential non linearity error(DNL)：±1LSB
Integral non linearity error(INL)：±1LSB
Signal-to-noise ratio distortion(SNR)：72.5dB @100 KHz
Total harmonic distortion(THD)：-83.5dB @100 KHz

Sampling rate 200 - 500 KSPS
SPI/ QSPI™/MICROWIRE ™/DSP serial interface
No pipeline cycle delay
Power saving mode
Unipolar single channel input, 0 V to VA range
6 Pin SOT-23 package

Ultra-low power consumption, power comparison with ADC101S021 (T=25℃):
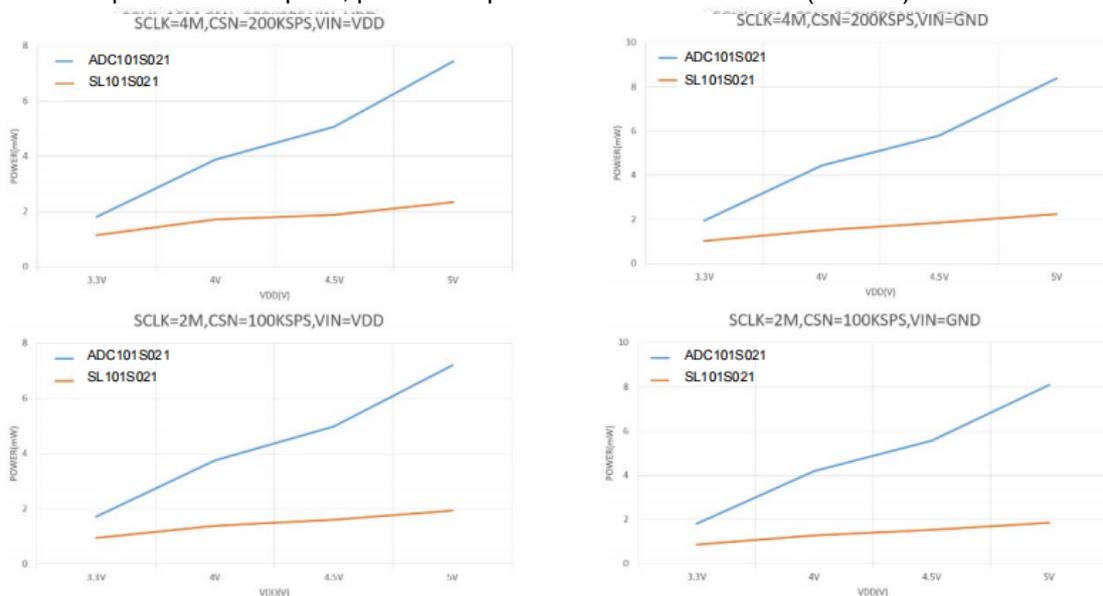

2.Pin configuration
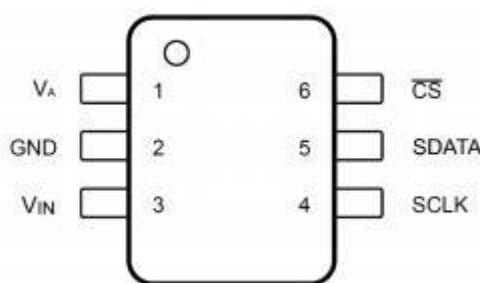
Pin diagram

| Pin		Description
Name	Serial number	
V_A	1	The power input is also similar to the reference voltage of the ADC.
GND	2	Analog input signal ground. All analog and digital signals are referenced to this pin.
V_{IN}	3	Analog signal input. Signal range is 0 V to V_A.
SCLK	4	Serial clock input. This clock directly controls the conversion and readout process.
SDATA	5	Serial data output.
CS	6	Chip select signal, low level is valid.

3.Typical connection

See the figure below for a typical connection circuit for the SL101S021. The power supply should come from a stable power supply device such as an LDO. The 1μF and 10nF coupling capacitors should be placed as close to the SL101S021 pins as possible. Always set the VA supply to be greater than or equal to the maximum V IN input signal to avoid maximum conversion code saturation.
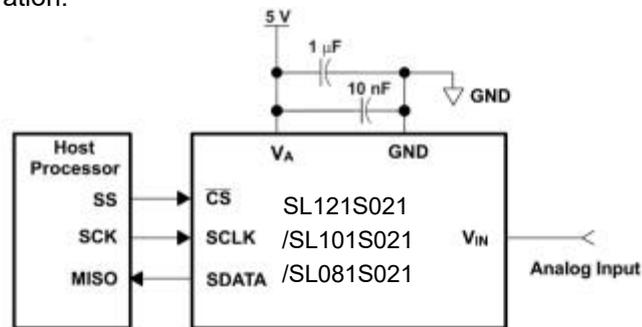
Circuit connection diagram

4.Timing diagram
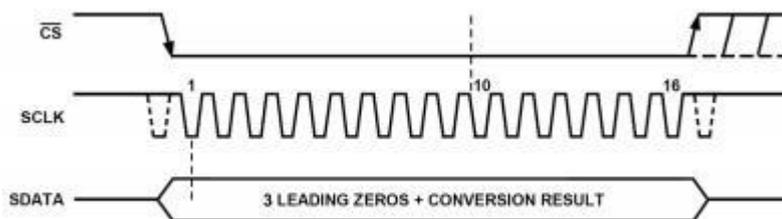
When the CS pin of SL101S021 is low and the serial clock SCLK signal is provided, SL101S021 can start a conversion cycle, as shown in the figure. The device outputs data during the conversion process, and the data is in MSB format. After 3 leading zeros, 12 bits of converted data are output. At the 16th falling edge of SCLK, SDATA enters the tri-state and the conversion cycle ends.
CS is pulled high after 16 clock SCLKs until the time 1μS after SDATA enters the tri-state ends. Pulling CS low again can start the next conversion.

5.Power saving mode

The SL12/10/081S021 series has an automatic power-down function. After shutting down all circuits, the converter usually consumes only a small current in this mode. When the CS falling edge appears, the device automatically wakes up. However, all functional blocks are fully enabled only when the third falling edge of SCLK appears. After the 16th falling edge of SCLK of SL101S021, the device detects the end of conversion and the device automatically powers down again. If CS is pulled high before 10 SCLKs, SL101S021 will terminate the ongoing data conversion process, the converter will be forced into power-down mode, and there will be no valid data in the next conversion.
The higher the SCLK frequency, the lower the power consumption of the converter at a fixed throughput rate, because the conversion time is shorter in a fixed period of time, that is, the converter is in automatic power-down mode more in each conversion cycle. For a specific SCLK frequency, the sampling time (CS falling edge to the third falling edge of SCLK) and conversion time (three leading zeros plus 8 SCLK cycles) are fixed, so lower throughput (i.e., longer total conversion cycle) increases the proportion of time that is powered off, thereby reducing power consumption.

6.Packaging diagram

TOP VIEW

RECOMMENDED LAND PATTERN

FRONT VIEW

SIDE VIEW

DETAIL "A"
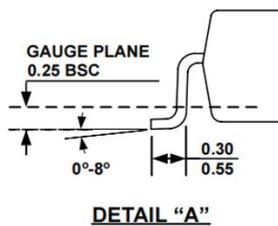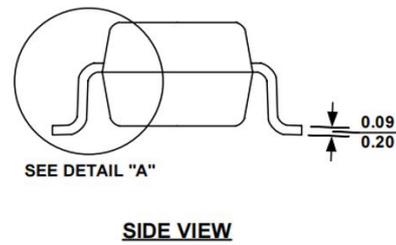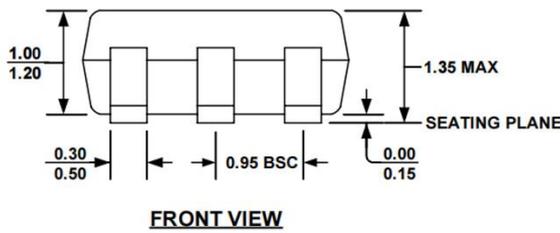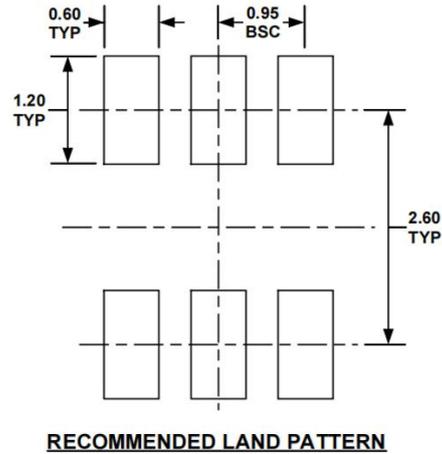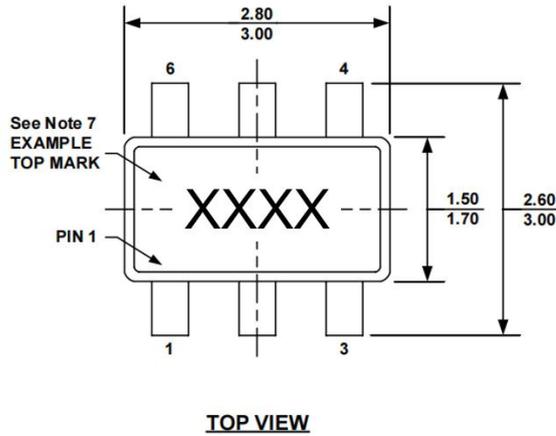
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

7.Precautions

1.Unpacked ICs and tube-packed ICs must be stored in a dry cabinet with a humidity of <20% R.H.

2.Components must be stored in anti-static packaging bags after storage and access.

3.Anti-static damage: The device is an electrostatic sensitive device. Adequate anti-static measures should be taken during transmission, assembly, and testing.

4.Users should conduct an appearance inspection before use. The bottom, sides, and surroundings of the circuit must be bright before welding. If oxidation occurs, the circuit can be treated by deoxidation means. After the treatment, the circuit must be welded within 12 hours.