12-bit high-resolution high-speed 3.3V-5.25V operating voltage 500-1000KSPS analog-to-digital converter (ADC)

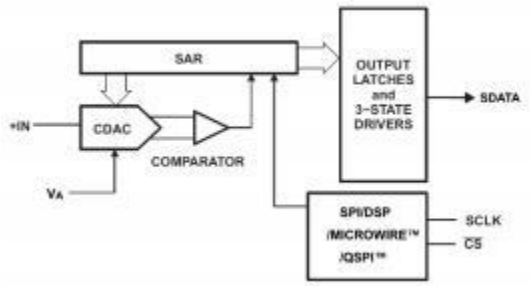
SL121S101 is a 12-bit ADC (Analog-to-Digital Converter) chip with the basic characteristics of high resolution, high speed, low power consumption, small size and unipolarity. The converter is based on a successive approximation register architecture with an internal sample-and-hold circuit. The converter is divided into two versions:
The SL121S101 version uses a single power supply of 4 V to 5.25 V, and its performance parameters cover 500KSPS to 800KSPS;
The SL121S101E version uses a single power supply of 3.3 V to 4.8 V, and its performance parameters cover 800KSPS to 1000KSPS. Both versions are currently packaged in a 6-pin SOT-23 package with an operating temperature range of -40℃ to 85℃.
SL121S101 can pin-to-pin replace ADC121S101, the dynamic power consumption at high voltage is less than 1/2, which significantly extends the battery operating time.

Main features

- SL121S101 sampling rate：500 – 800 KSPS
  SL121S101E sampling rate：800 – 1000 KSPS
- SL121S101 voltage range：4 V to 5.25 V
  SL121S101E voltage range：3.3V to4.8 V
- 12-bit resolution
- Low power（SL121S101 typical value） 6.05mW（5V，800 KSPS）3.60mW（4V，800 KSPS）
- Maximum deviation ±1.25LSB INL，±1LSB DNL
- 0—VA unipolar single channel input
- SPI, QSPI™, MICROWIRE™, DSP serial Interface
- 6 pinSOT-23 package

Application Areas

- Portable systems
- Remote data collection
- Instrumentation and control systems
- Optical sensors
- Battery powered system



Schematic

Packaging effect diagram

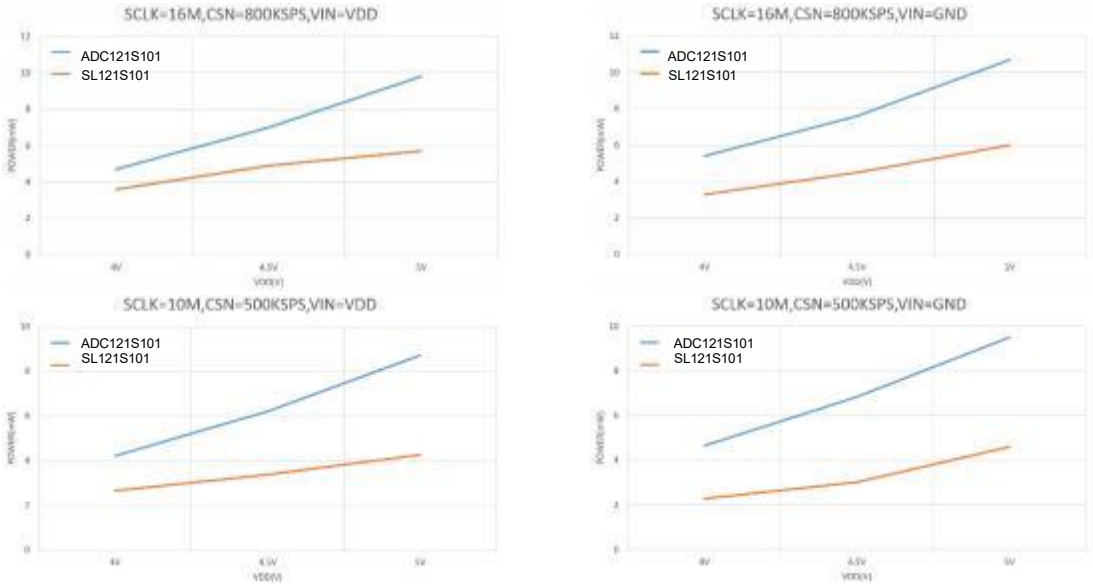
Pin-compatible resolution and speed alternative

Resolution	Specify the sampling rate range			
	50 to 200 KSPS	200 to 500 KSPS	500 to 800 KSPS	800 to 1000 KSPS
12-bit	SL121S021	SL121S051	SL121S101	SL121S101E
10-bit	SL101S021	SL101S051	SL101S101	SL101S101E
8-bit	SL081S021	SL081S051	SL081S101	SL081S101E

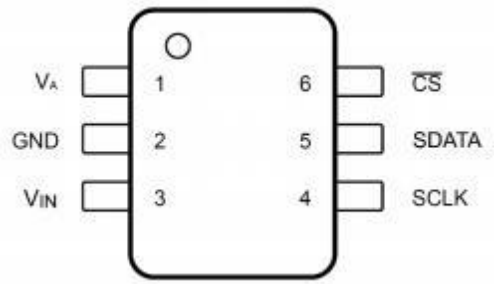
1.Main technical parameters

- SL121S101 ： 4V to 5.25V single power supply
  SL121S101E ： 3.3V to4.8V single power supply
- 12-bit resolution, no missing codes
- Differential non linearity error (DNL)：±1LSB
- Integral non linearity error (INL)：±1.25LSB
- Signal-to-noise ratio distortion (SNR)：72.5dB @100 KHz
- Total harmonic distortion (THD)：-81dB @100 KHz
- SL121S101 sampling rate：500 – 800 KSPS
  SL121S101E sampling rate：800 – 1000 KSPS
- SPI/QSPI™/MICROWIRE™/DSP compatible with serial interface
- No pipeline cycle delay
- Power saving mode
- Unipolar single channel input, 0 V to VA range
- 6 Pin SOT-23 package

Ultra-low power consumption, power comparison with ADC121S101 (T=25℃):



2.Pin configuration

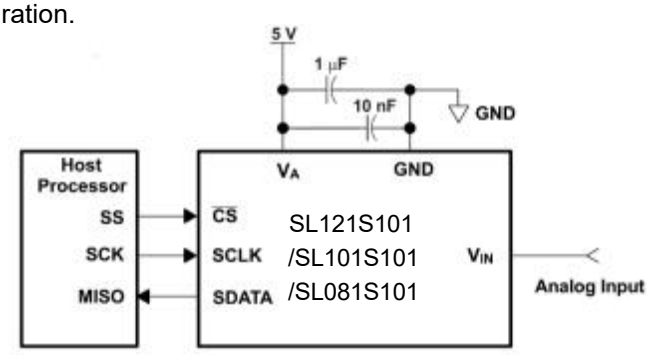


Pin diagram

Pin		Description
Name	Serial number	
V_A	1	The power input is also similar to the reference voltage of the ADC.
GND	2	Analog input signal ground. All analog and digital signals are referenced to this pin.
V_{IN}	3	Analog signal input. Signal range is 0 V to V_A.
SCLK	4	Serial clock input. This clock directly controls the conversion and readout process.
SDATA	5	Serial data output.
CS	6	Chip select signal, low level is valid.

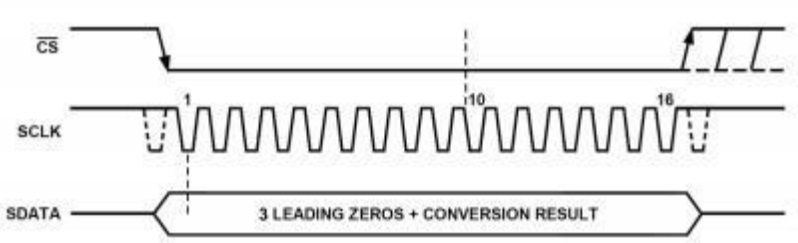
3.Typical connection

See the figure below for a typical connection circuit for the SL121S101. The power supply should come from a stable power supply device such as an LDO. The 1μF and 10nF coupling capacitors should be placed as close to the SL121S101 pins as possible. Always set the VA supply to be greater than or equal to the maximum V IN input signal to avoid maximum conversion code saturation.



Circuit connection diagram

4.Timing diagram

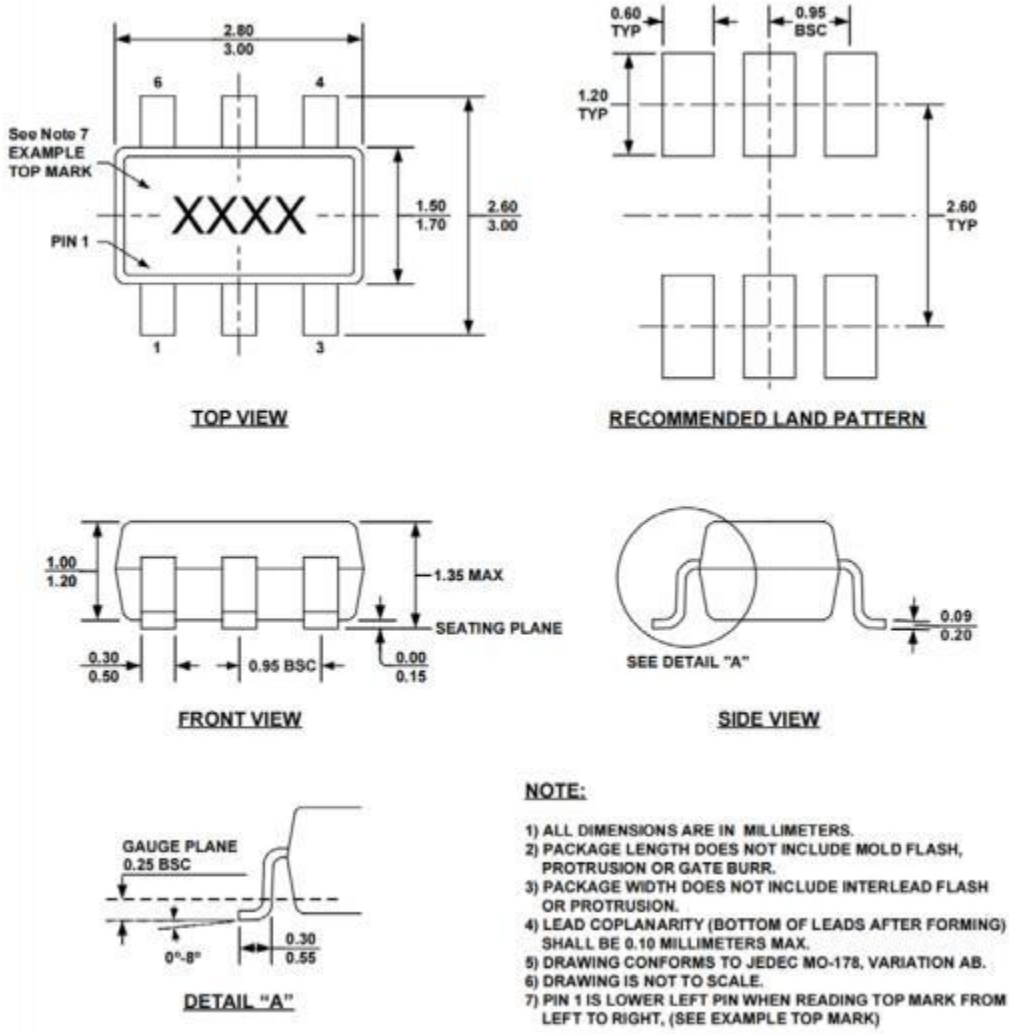


When the CS pin of SL121S101 is low and the serial clock SCLK signal is provided, SL121S101 can start a conversion cycle, as shown in the figure. The device outputs data during the conversion process, and the data is in MSB format. After 3 leading zeros, 12 bits of converted data are output. At the 16th falling edge of SCLK, SDATA enters the tri-state and the conversion cycle ends.
CS is pulled high after 16 clock SCLKs until the time 1μS after SDATA enters the tri-state ends. Pulling CS low again can start the next conversion.

5.Power saving mode

The SL12/10/081S101 series has an automatic power-down function. After shutting down all circuits, the converter usually consumes only a small current in this mode. When the CS falling edge appears, the device automatically wakes up. However, all functional blocks are fully enabled only when the third falling edge of SCLK appears. After the 16th falling edge of SCLK of SL121S101, the device detects the end of conversion and the device automatically powers down again. If CS is pulled high before 10 SCLKs, SL121S101 will terminate the ongoing data conversion process, the converter will be forced into power-down mode, and there will be no valid data in the next conversion.
The higher the SCLK frequency, the lower the power consumption of the converter at a fixed throughput rate, because the conversion time is shorter in a fixed period of time, that is, the converter is in automatic power-down mode more in each conversion cycle. For a specific SCLK frequency, the sampling time (CS falling edge to the third falling edge of SCLK) and conversion time (three leading zeros plus 12 SCLK cycles) are fixed, so lower throughput (i.e., longer total conversion cycle) increases the proportion of time that is powered off, thereby reducing power consumption.

6.Packaging diagram



7.Precautions

1.Unpacked ICs and tube-packed ICs must be stored in a dry cabinet with a humidity of <20% R.H.

2.Components must be stored in anti-static packaging bags after storage and access.

3.Anti-static damage: The device is an electrostatic sensitive device. Adequate anti-static measures should be taken during transmission, assembly, and testing.

4.Users should conduct an appearance inspection before use. The bottom, sides, and surroundings of the circuit must be bright before welding. If oxidation occurs, the circuit can be treated by deoxidation means. After the treatment, the circuit must be welded within 12 hours.