

12-bit high-resolution high-speed 1.5V-4.5V operating voltage 200KSPS-1MSPS analog-to-digital converter (ADC)

Description

SL7866 is a 12-bit ADC (Analog-to-Digital Converter) chip, which has the basic characteristics of ultra-low power consumption, small size, unipolarity, and single-ended input. SL7866 is designed with advanced process and technology and has a wide voltage operating range:

When powered by a single 1.5V-3.0V power supply, the sampling rate can reach up to 200KSPS (compatible with similar chips); when powered by a single 3.0V-4.5V power supply, the sampling rate can reach up to 1MSPS.

The SL7866 uses a 6-pin SOT-23 package and has an operating temperature range of -40 to 85.

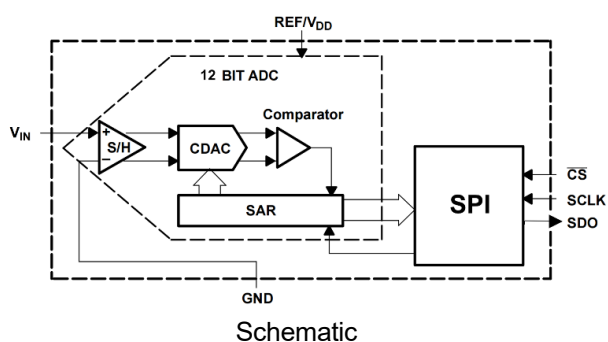
The SL7866 is a pin-to-pin replacement for the ADS7866 and consumes less than one-third of the dynamic power, significantly extending battery life.

Features

- Maximum sampling rate: 200 KSPS (1.5V-3V)
- Maximum sampling rate: 1250 KSPS
- Ultra-low power consumption (typical)
 - 0.13mW (1.8V, 200 KSPS)
 - 0.62mW (3.3V, 200 KSPS)
- Maximum error $\pm 1.5\text{LSB INL}$, $\pm 1.5\text{LSB DNL}$
- 0-VDD unipolar single channel input
- SPI compatible serial interface
- 6-pin SOT-23 package

Application

- Battery-powered systems
- Portable communication equipment
- Medical electronic equipment
- Portable data acquisition equipment
- Internet of Things data acquisition equipment
- Automatic measuring instruments



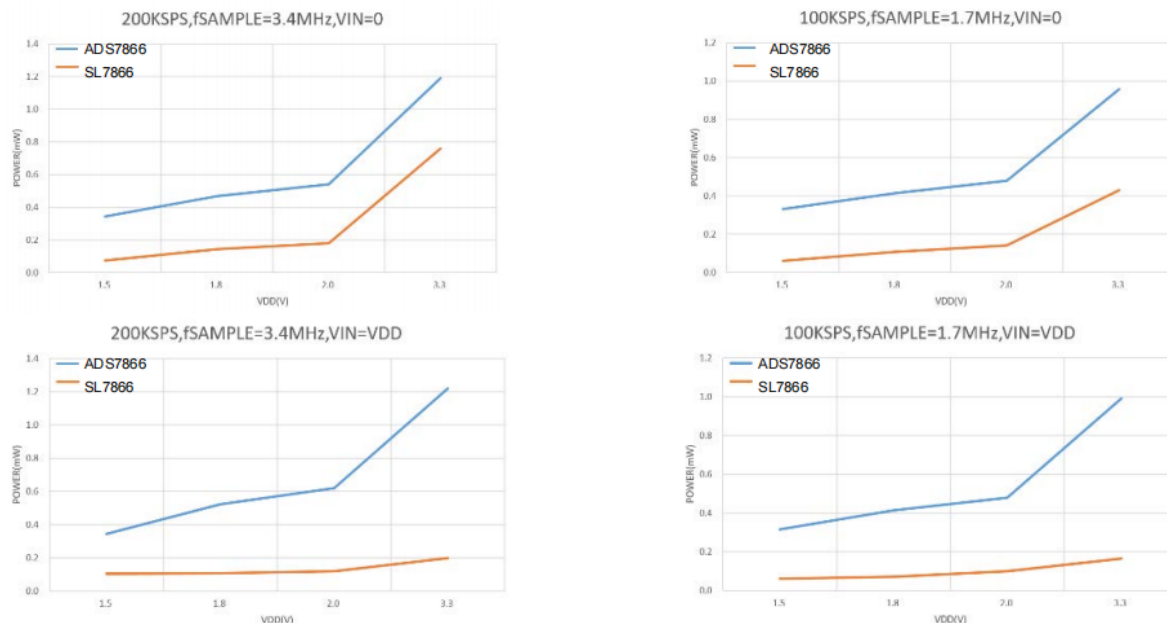
Packaging diagram

1. Main technical parameters

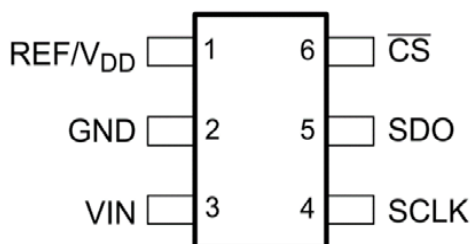
1.5V-4.5V single power supply
 12-bit resolution, no missing codes
 Differential nonlinearity error (DNL): ± 1.5 LSB
 Integral nonlinearity error (INL): ± 1.5 LSB
 Signal-to-noise ratio distortion (SNR): 71.25 dB @30 KHz
 Total harmonic distortion (THD): -84 dB @30 KHz
 Unipolar single channel input, 0 V to VDD range

Maximum sampling rate 200 KSPS (1.5V-3.0V)
 Maximum sampling rate 1 MSPS (3.0V-4.5V)
 SPI-compatible serial interface
 No pipeline cycle delay
 Automatic shutdown
 6-pin SOT-23 package

Power comparison with ADS7866(T=25°C):



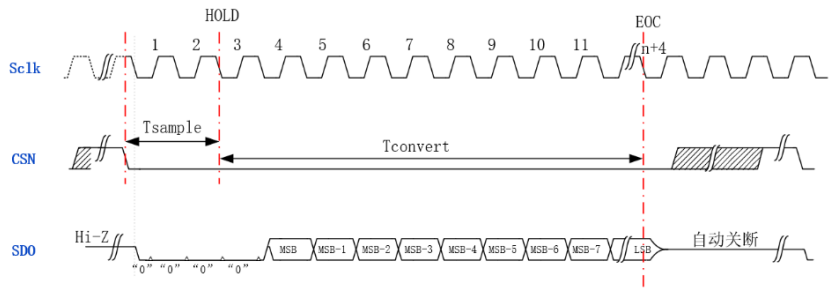
2. Pin configuration



Pin diagram

Pin		Description
Name	Serial number	
REF/V _{DD}	1	External reference input and power supply.
GND	2	Analog input signal ground. All analog and digital signals are referenced to this pin.
V _{IN}	3	Analog signal input. Signal range is 0 V to V _A .
SCLK	4	Serial clock input. This clock directly controls the conversion and readout process.
SDATA	5	Serial data output.
CS	6	Chip select signal, low level is valid.

3. Timing diagram

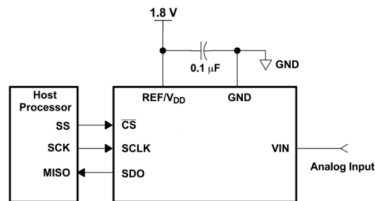


n=12

A conversion cycle is initiated when the CS pin is pulled low and the serial clock SCLK signal is provided. After the CS falling edge, the time between the 3rd falling edge of SCLK (T_{sample}) is used to sample the input signal. After the 3rd SCLK falling edge, the ADC enters the hold mode/conversion cycle ($T_{convert}$) and begins the digitization process of the sampled input signal. At the 16th falling edge of SCLK, SDO enters the high impedance state and the conversion cycle ends.

4. Typical connection

See the figure below for a typical connection circuit of the SL7866. The 1.8V power supply should come from a stable power supply device, such as an LDO. A 0.1 μF coupling capacitor is required between the REF/VDD pin and the GND pin of the SL7866. The capacitor should be as close to the pin of the SL7866 as possible.



Circuit connection diagram

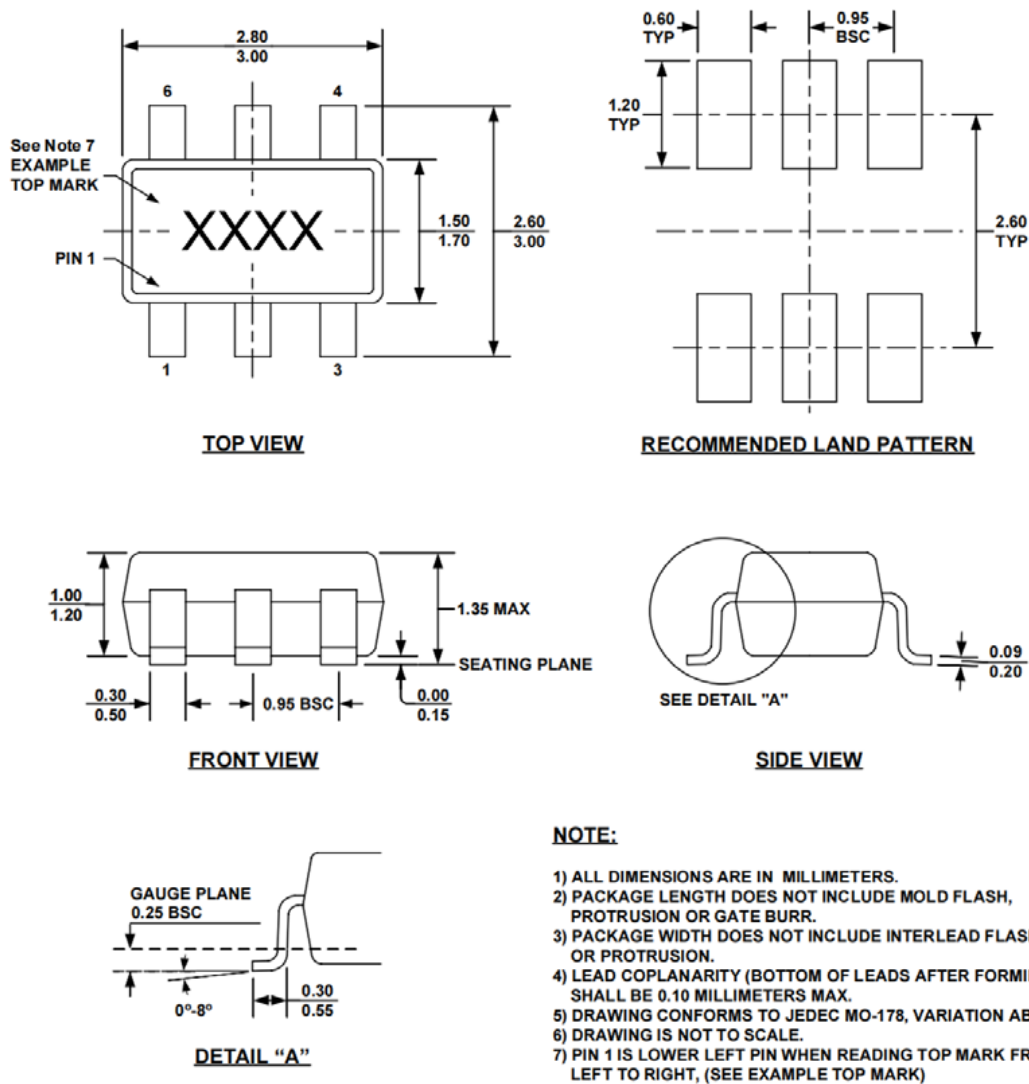
5. Conversion results

Description	Analog input voltage	Digital output system	
		Binary	Hexadecimal
SL7866(12 bit)			
Least Significant Bit(LSB)	$V_{DD}/4096$		
Full Scale	$V_{DD}-1LSB$	111111111111	FFF
Mid Scale	$V_{DD}/2$	100000000000	800
Mid Scale-1LSB	$V_{DD}/2-1LSB$	011111111111	7FF
Zero	0V	000000000000	000

The SL7866 outputs 12 bits of converted data after 4 leading zeros, and these codes are in standard binary format.

After power-up, the SL7866 has no specific initialization requirements, but the first conversion will not produce valid results. To set the SL7866 to a known state, CS is changed from low to high after VDD stabilizes during power-up. This places the SL7866 in auto-shutdown mode, and the serial data output (SDO) is high impedance. The next time the CS pin is lowered and the serial clock SCLK signal is provided, the conversion can be performed normally and the result can be output.

6. Packaging diagram



7. Precautions

1. Unpacked ICs and tube-packed ICs must be stored in a dry cabinet with a humidity of <20% R.H.
2. Components must be stored in anti-static packaging bags after storage and access.
3. Anti-static damage: The device is an electrostatic sensitive device. Adequate anti-static measures should be taken during transmission, assembly, and testing.
4. Users should conduct an appearance inspection before use. The bottom, sides, and surroundings of the circuit must be bright before welding. If oxidation occurs, the circuit can be treated by deoxidation means. After the treatment, the circuit must be welded within 12 hours.