8-bit high-resolution high-speed 1.5V-4.5V operating voltage 280KSPS-1.4 MSPS analog-to-digital converter (ADC)

Description

SL7868 is a 8-bit ADC (Analog-to-Digital Converter) chip, which has the basic characteristics of ultra-low power consumption, small size, unipolarity, and single-ended input. SL7868 is designed with advanced process and technology and has a wide voltage operating range:

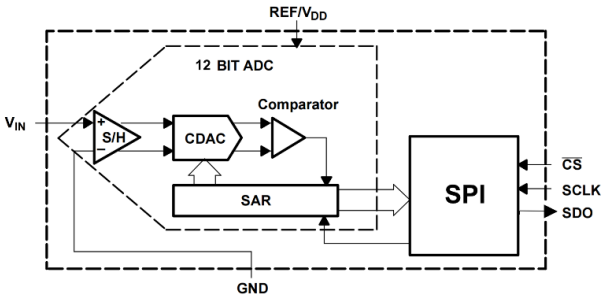
When powered by a single 1.5V-3.0V power supply, the sampling rate can reach up to 280KSPS (compatible with similar chips); when powered by a single 3.0V-4.5V power supply, the sampling rate can reach up to 1.4MSPS.
The SL7868 uses a 6-pin SOT-23 package and has an operating temperature range of -40 to 85.
The SL7868 is a pin-to-pin replacement for the ADS7868 and consumes less than one-third of the dynamic power, significantly extending battery life.

Features

- 1.5V-4.5V single supply voltage with automatic power-off.
- Maximum sampling rate: 280 KSPS (1.5V-3V)
  Maximum sampling rate: 1.4 MSPS (3.0V-4.5V)
- Ultra-low power consumption (typical)
  0.16mW (1.8V, 280 KSPS)
  0.48mW (3.3V, 280 KSPS)
- Maximumerror±0.5LSBINL,±0.5LSBDNL
- 0-VDD unipolar single channel input
- SPI compatible serial interface
- 6-pin SOT-23 package

Application

- Battery-powered systems
- Portable communication equipment
- Medical electronic equipment
- Portable data acquisition equipment
- Internet of Things data acquisition equipment
- Automatic measuring instruments



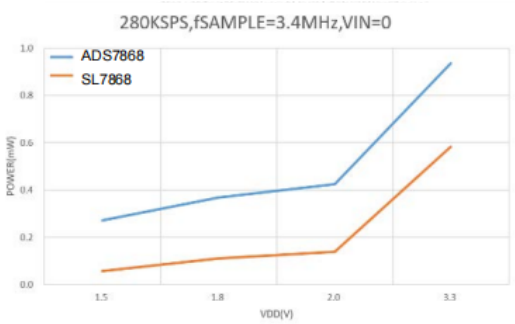
Schematic

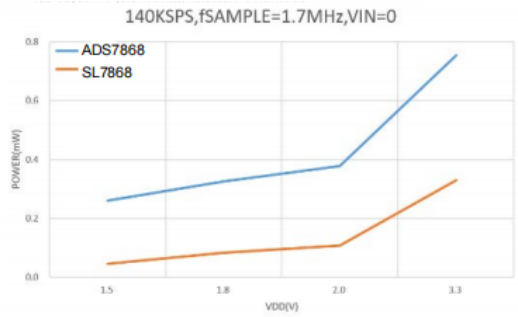
Packaging diagram

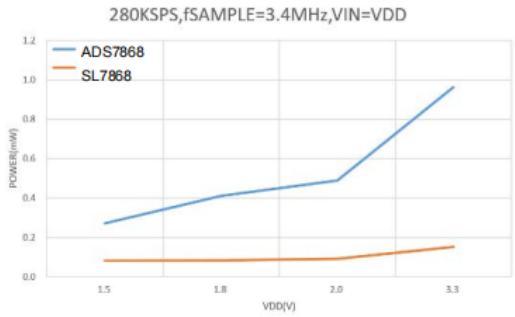
1.Main technical parameters

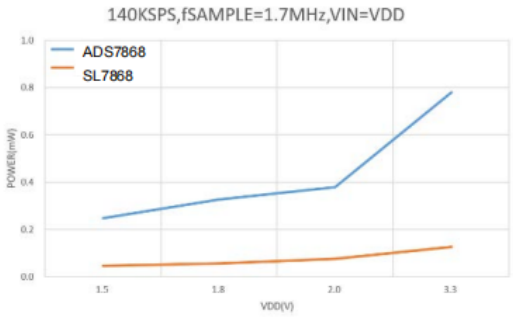
- 1.5V-4.5V single power supply
- 8-bit resolution, no missing codes
- Differential nonlinearity error (DNL): ±0.5LSB
- Integral nonlinearity error (INL): ±0.5LSB
- Signal-to-noise ratio distortion (SNR): 49.5 dB @30 KHz
- Total harmonic distortion (THD): -70 dB @30 KHz
- Unipolar single channel input, 0 V to VDD range
- Maximum sampling rate 280 KSPS (1.5V-3.0V)
- Maximum sampling rate 1.4 MSPS (3.0V-4.5V)
- SPI-compatible serial interface
- No pipeline cycle delay
- Automatic power-off
- 6-pin SOT-23 package

Power comparison with ADS7868(T=25℃):

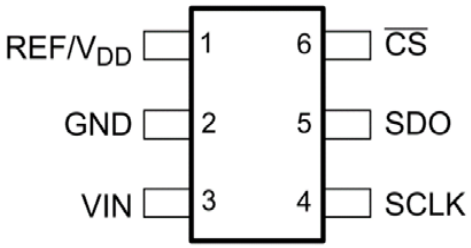








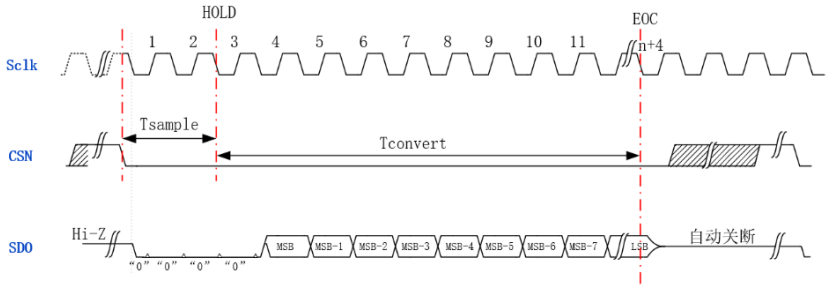
2.Pin configuration



Pin diagram

Pin		Description
Name	Serial number	
REF/V_{DD}	1	External reference input and power supply.
GND	2	Analog input signal ground. All analog and digital signals are referenced to this pin.
V_{IN}	3	Analog signal input. Signal range is 0 V to V_A.
SCLK	4	Serial clock input. This clock directly controls the conversion and readout process.
SDATA	5	Serial data output.
CS	6	Chip select signal, low level is valid.

3.Timing diagram

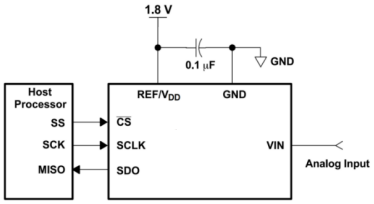


n=8

A conversion cycle is initiated when the CS pin is pulled low and the serial clock SCLK signal is provided. After the CS falling edge, the time between the 3rd falling edge of SCLK (Tsample) is used to sample the input signal. After the 3rd SCLK falling edge, the ADC enters the hold mode/conversion cycle (Tconvert) and begins the digitization process of the sampled input signal. At the 16th falling edge of SCLK, SDO enters the high impedance state and the conversion cycle ends.

4.Typical connection

See the figure below for a typical connection circuit of the SL7868. The 1.8V power supply should come from a stable power supply device, such as an LDO. A 0.1 μF coupling capacitor is required between the REF/VDD pin and the GND pin of the SL7868. The capacitor should be as close to the pin of the SL7868 as possible.



Circuit connection diagram

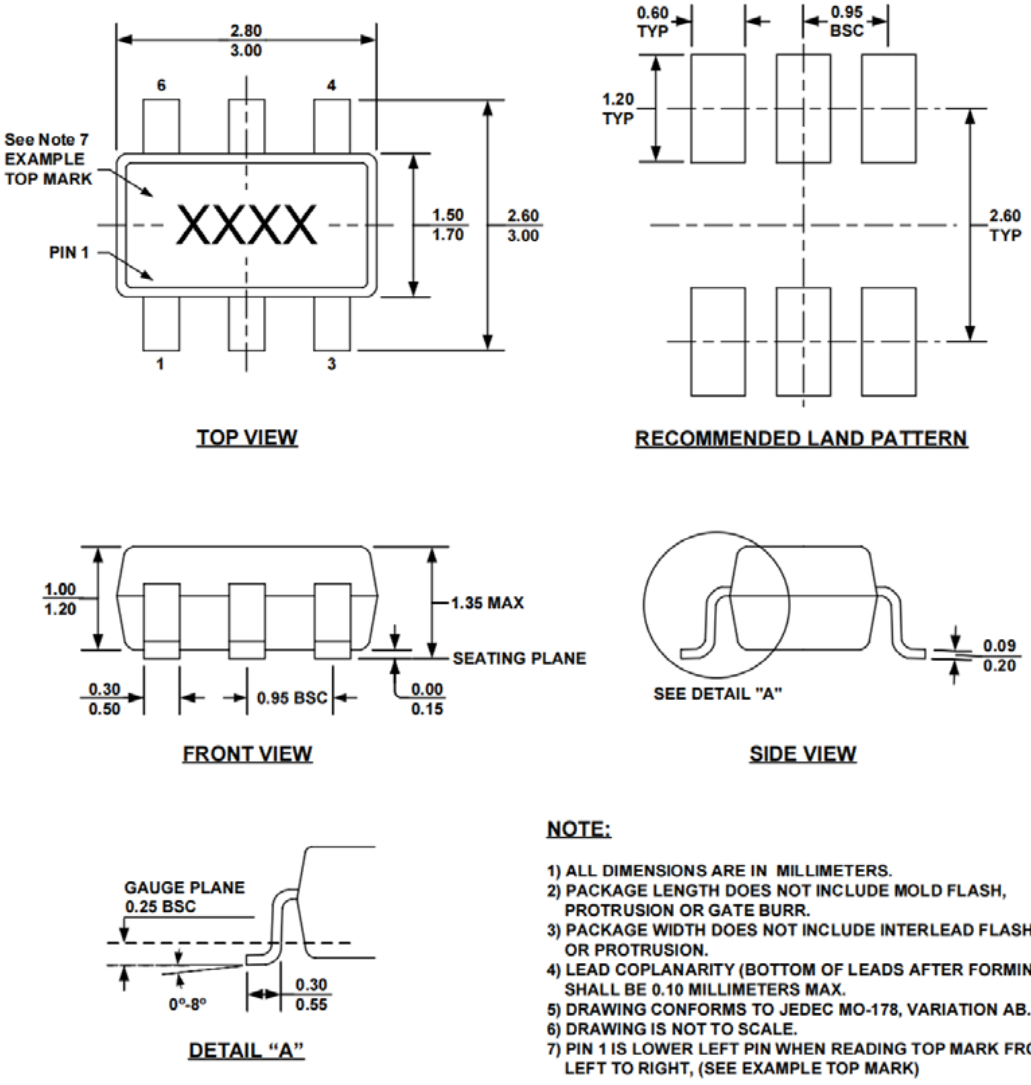
5.Conversion results

Description	Analog input voltage	Digital output system	
		Binary	Hexadecimal
SL7868(12 bit)			
Least Significant Bit(LSB)	V_{DD}/256		
Full Scale	V_{DD}-1LSB	111111111111	FF
Mid Scale	V_{DD}/2	100000000000	80
Mid Scale-1LSB	V_{DD}/2-1LSB	011111111111	7F
Zero	0V	000000000000	00

The SL7868 outputs 10 bits of converted data after 4 leading zeros, and these codes are in standard binary format.

After power-up, the SL7868 has no specific initialization requirements, but the first conversion will not produce valid results. To set the SL7868 to a known state, CS is changed from low to high after VDD stabilizes during power-up. This places the SL7868 in auto-shutdown mode, and the serial data output (SDO) is high impedance. The next time the CS pin is lowered and the serial clock SCLK signal is provided, the conversion can be performed normally and the result can be output.

6.Packaging diagram



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

7.Precautions

1.Unpacked ICs and tube-packed ICs must be stored in a dry cabinet with a humidity of <20% R.H.

2.Components must be stored in anti-static packaging bags after storage and access.

3.Anti-static damage: The device is an electrostatic sensitive device. Adequate anti-static measures should be taken during transmission, assembly, and testing.

4.Users should conduct an appearance inspection before use. The bottom, sides, and surroundings of the circuit must be bright before welding. If oxidation occurs, the circuit can be treated by deoxidation means. After the treatment, the circuit must be welded within 12 hours.