12-bit high-resolution high-speed 3.3V-5.25V operating voltage 1000KSPS analog-to-digital converter (ADC)

Description

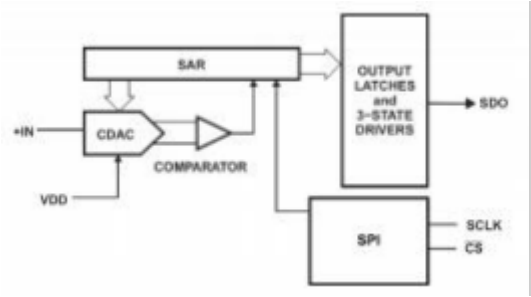
SL7886 is a 12-bit ADC (Analog-to-Digital Converter) chip, which has the basic characteristics of high resolution, high speed, low power consumption, small size and uni polarity. The product is divided into two versions:
The SL7886 version is powered by a single power supply of 4 V-5.25 V, and the sampling rate can reach up to 800 KSPS. The SL7886E version is powered by a single power supply of 3.3 V-4.8 V, and the sampling rate can reach up to 1000 KSPS. Both versions are packaged in a 6-pin SOT-23 package with an operating temperature range of -40 to 85.
SL7886 is a pin-to-pin replacement for ADS7886 with less than 1/2 of the average dynamic power consumption, significantly extending the battery operating time.

Features

- SL7886 maximum sampling rate: 800 KSPS
- SL7886E maximum sampling rate: 1000 KSPS
- 4 V—5.25 V single power supply(SL7886)
  3.3 V—4.8 V Single power supply(SL7886E)
- 12-bit resolution
- Supply voltage range: 3.3V to 5.25V
- Up to 20MHz serial interface(SL7886E)
- Low power（typical value）
  6.05mW（5V，800 KSPS）
  3.50mW（4V，800 KSPS）
- Maximum error ±1.5LSB INL，±1.25LSB DNL
- Power saving mode
- 6 pin SOT-23 package

Application

- Baseband converters in wireless communications
- Motor current and bus voltage sensors in digital drives
- Optical networks (DWDM, MEMS-based switches)
- Optical sensors
- Battery powered system
- Medical devices
- High-speed data acquisition system
- High-speed closed-loop system



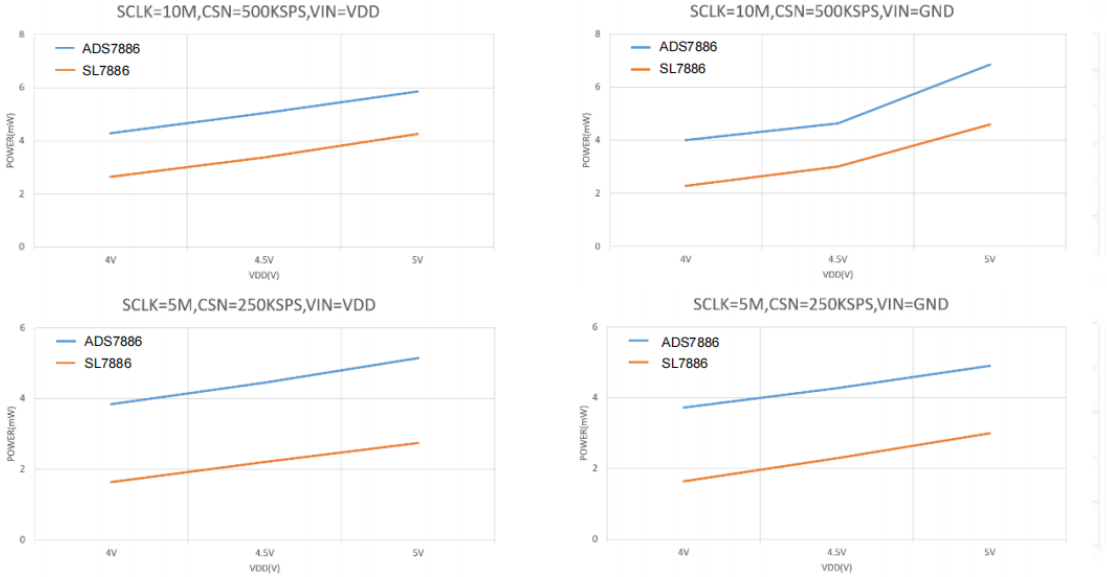
Schematic

Packaging effect diagram

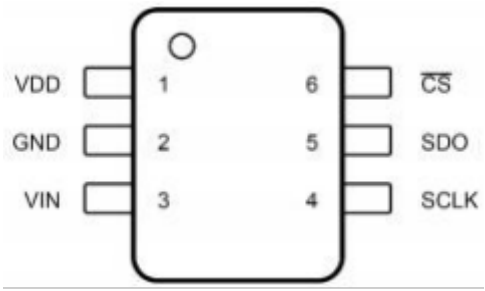
1.Main technical parameters

- 4 V—5.25 V Single power supply(SL7886)
- 3.3 V—4.8 V Single power supply(SL7886E)
- 12-bit resolution, no missing codes
- Differential non linearity error(DNL)：±1.25LSB
- Integral non linearity error(INL)：±1.5LSB
- Signal-to-noise ratio distortion(SNR)：72.5dB @100 KHz
- Total harmonic distortion(THD)：-84.5dB @100 KHz
- SL7886 Maximum Sampling rate 800 KSPS
  SL7886E Maximum Sampling rate 1000 KSPS
- SPI/ QSPI™/MICROWIRE ™/DSP serial interface
- No pipeline cycle delay
- Power saving mode
- Unipolar single channel input, 0 V to V_{DD} range
- 6 Pin SOT-23 package

Ultra-low power consumption, power comparison with ADS7886(T=25℃):



2.Pin configuration

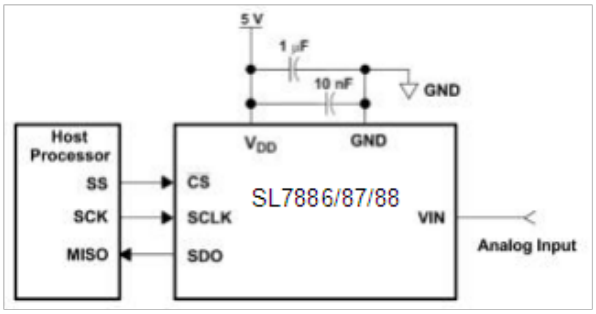


Pin diagram

Pin		Description
Name	Serial number	
V_{DD}	1	The power input is also similar to the reference voltage of the ADC.
GND	2	Analog input signal ground. All analog and digital signals are referenced to this pin.
V_{IN}	3	Analog signal input. Signal range is 0 V to V_A.
SCLK	4	Serial clock input. This clock directly controls the conversion and readout process.
SDATA	5	Serial data output.
CS	6	Chip select signal, low level is valid.

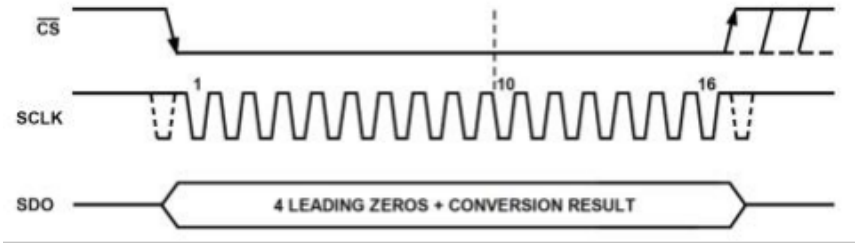
3.Typical connection

See the figure below for a typical connection circuit for SL7886. The power supply should come from a stable power supply device such as an LDO. The 1μF and 10nF coupling capacitors should be placed as close to the SL7886 pins as possible. Always set the VDD power supply to be greater than or equal to the maximum VIN input signal to avoid maximum conversion code saturation.



Circuit connection diagram

4.Timing diagram

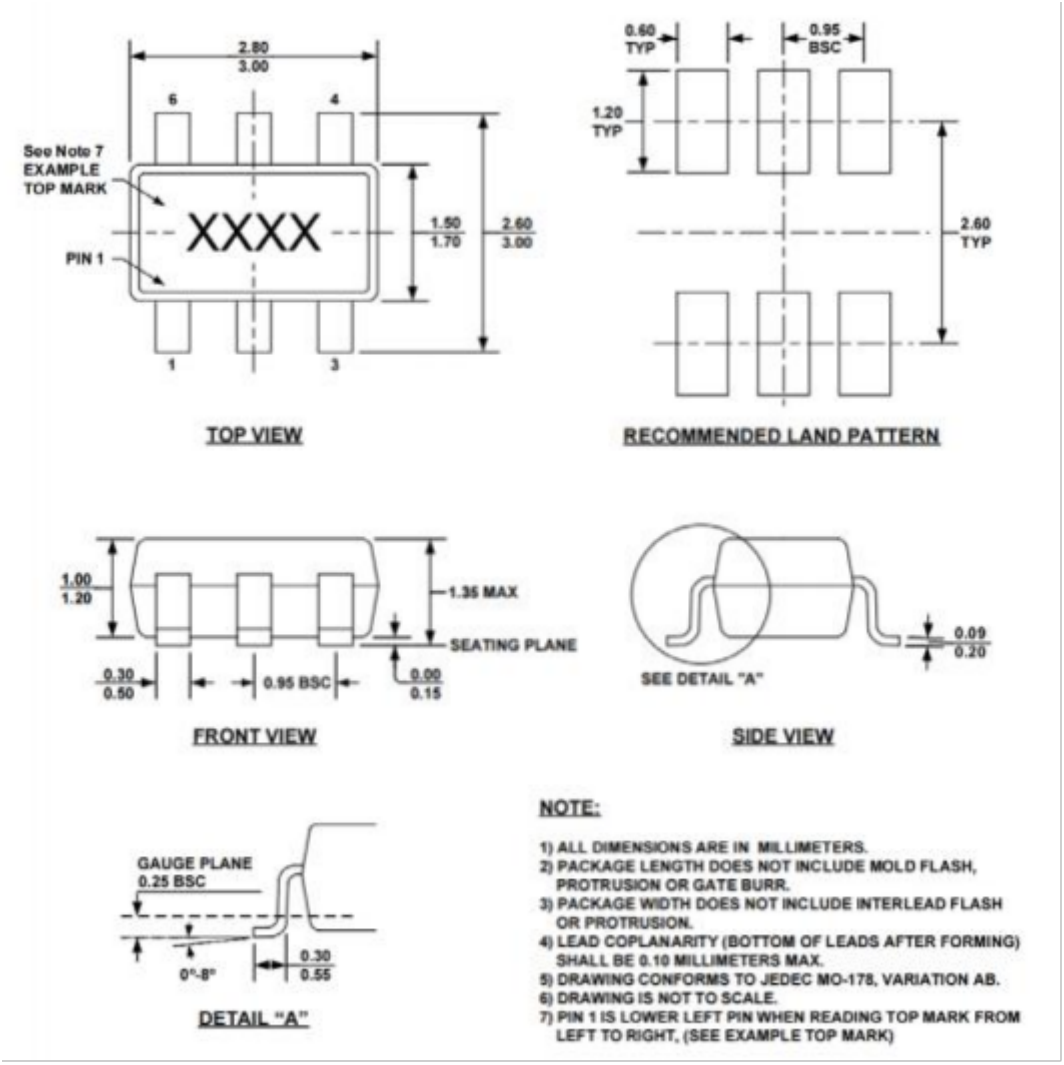


When the CS pin of SL7886 is low and the serial clock SCLK signal is provided, SL7886 can start a conversion cycle, as shown in the figure. The device outputs data during the conversion process, and the data is in MSB format. After 4 leading zeros, 12 bits of converted data are output. At the 16th falling edge of SCLK, SDATA enters the tri-state and the conversion cycle ends.
CS is pulled high after 16 clock SCLKs until the time 1μS after SDATA enters the tri-state ends. Pulling CS low again can start the next conversion.

5.Power saving mode

The SL7886/87/88 series has an automatic power-down function. After shutting down all circuits, the converter usually consumes only a small current in this mode. When the CS falling edge appears, the device automatically wakes up. However, all functional blocks are fully enabled only when the third falling edge of SCLK appears. After the 16th falling edge of SCLK of SL7886, the device detects the end of conversion and the device automatically powers down again. If CS is pulled high before 10 SCLKs, SL7886 will terminate the ongoing data conversion process, the converter will be forced into power-down mode, and there will be no valid data in the next conversion.
The higher the SCLK frequency, the lower the power consumption of the converter at a fixed throughput rate, because the conversion time is shorter in a fixed period of time, that is, the converter is in automatic power-down mode more in each conversion cycle. For a specific SCLK frequency, the sampling time (CS falling edge to the third falling edge of SCLK) and conversion time (three leading zeros plus 12 SCLK cycles) are fixed, so lower throughput (i.e., longer total conversion cycle) increases the proportion of time that is powered off, thereby reducing power consumption.

6.Packaging diagram



7.Precautions

1.Unpacked ICs and tube-packed ICs must be stored in a dry cabinet with a humidity of <20% R.H.

2.Components must be stored in anti-static packaging bags after storage and access.

3.Anti-static damage: The device is an electrostatic sensitive device. Adequate anti-static measures should be taken during transmission, assembly, and testing.

4.Users should conduct an appearance inspection before use. The bottom, sides, and surroundings of the circuit must be bright before welding. If oxidation occurs, the circuit can be treated by deoxidation means. After the treatment, the circuit must be welded within 12 hours.