12-bit high-resolution high-speed 3.3V-5.25V operating voltage 1MSPS analog -to-digital converter (ADC)

Description

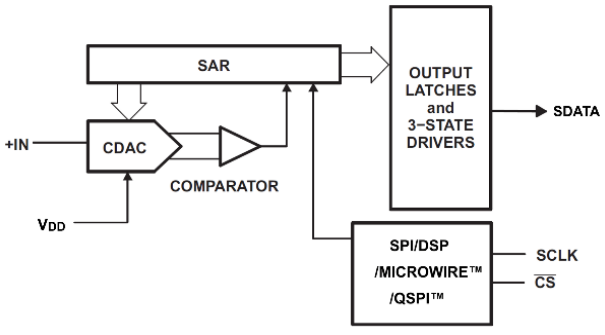
SLS7476 is a 12-bit ADC (Analog-to-Digital Converter) chip, which has the basic characteristics of high resolution, high speed, low power consumption, small size and unipolarity. The product is divided into two versions: SLS7476 version is powered by a single power supply of 4V-5.25V, and the sampling rate can reach up to 800 KSPS. SL S7476E version is powered by a single power supply of 3.3V-4.8V, and the sampling rate can reach up to 1 MSPS. Both versions are packaged in 6-pin SOT-23 and have an operating temperature range of -40℃ to 85℃.
The SLS7476 is a pin-to-pin replacement for the ADCS7476 and consumes less than 1/2 the dynamic power at high voltage, significantly extending battery operating time.

Features

- SLS7476 Maximum sampling rate: 800 KSPS
- SLS7476E Maximum sampling rate: 1 MSPS
- 12-bit resolution
- 4 V-5.25 V single power supply (SLS7476)
- 3.3 V-4.8 V single power supply (SLS7476E)
- Low power consumption (SLS7476 typical)
- 6.1 mW (5 V, 800 KSPS)
- 3.4 mW (4 V, 800 KSPS)
- Maximum error ±1.25 LSB INL, ±1.25 LSB DNL
- SPI/DSP/MICROWIRE™/QSPI™ serial interface
- Power-saving mode
- 6-pin SOT-23 package

Application

- Car navigation
- Automatic telephone or ATM equipment
- Portable systems
- Medical devices
- Mobile communications
- Battery-powered systems
- Instrumentation and control systems



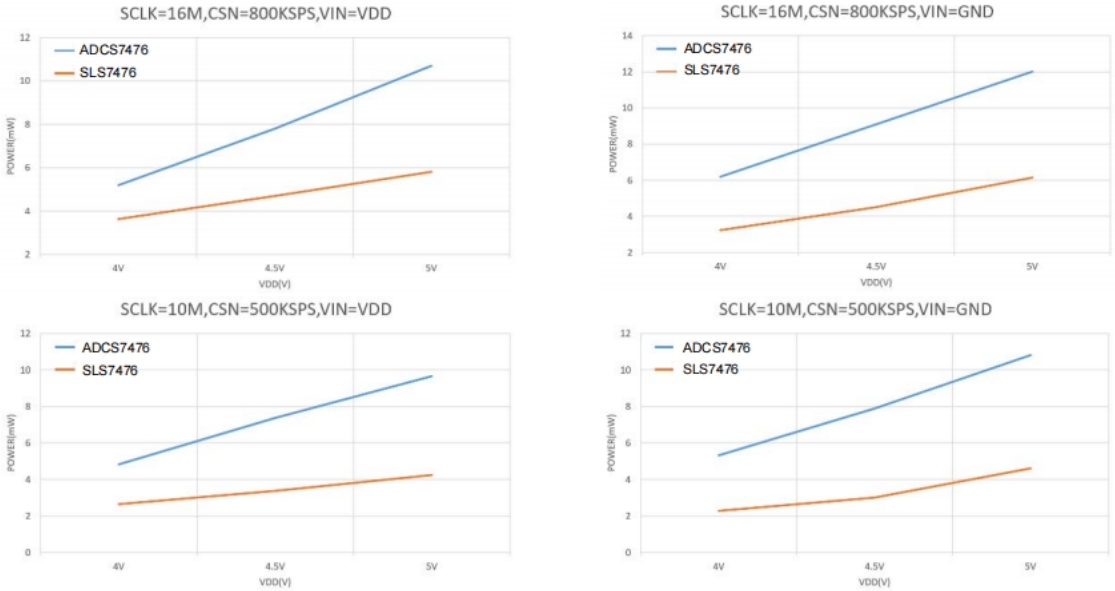
Schematic

Packaging diagram

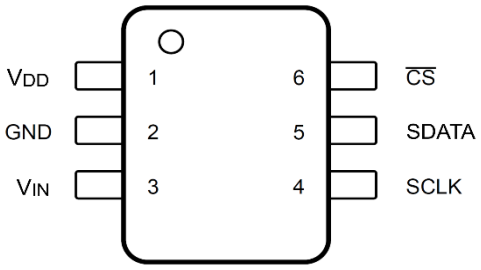
1.Main technical parameters

- 4 V—5.25 V single power supply (SLS7476)
- 3.3 V—4.8 V single power supply (SLS7476E)
- 12-bit resolution, no missing codes
- Differential nonlinearity error (DNL): ±1. 25LSB
- Integral nonlinearity error (INL): ±1.25LSB
- SNR: 71.5dB @100 KHz
- Total harmonic distortion (THD): -84dB @ 100 KHz
- SLS7476 Maximum sampling rate: 800 KSPS
- SLS7476E Maximum sampling rate: 1 MSPS
- SPI/DSP/MICROWIRE™/QSPI™ compatible serial interface
- No pipeline cycle delay
- Power saving mode
- Unipolar single channel input, 0 V to VDD range
- 6-pin SOT-23 package

Power comparison with ADC7476(T=25℃):



2.Pin configuration

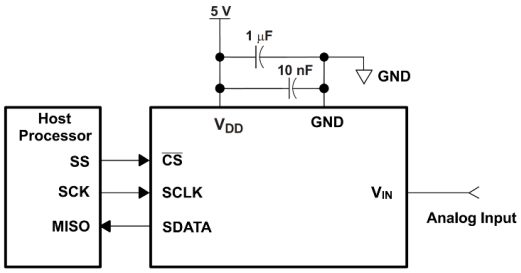


Pin diagram

Pin		Description
Name	Serial number	
V_{DD}	1	Power supply input, also similar to the reference voltage of the ADC.
GND	2	Analog input signal ground. All analog and digital signals are referenced to this pin.
V_{IN}	3	Analog signal input. Signal range is 0 V to V_A.
SCLK	4	Serial clock input. This clock directly controls the conversion and readout process.
SDATA	5	Serial data output.
CS	6	Chip select signal, low level is valid.

3.Typical connection

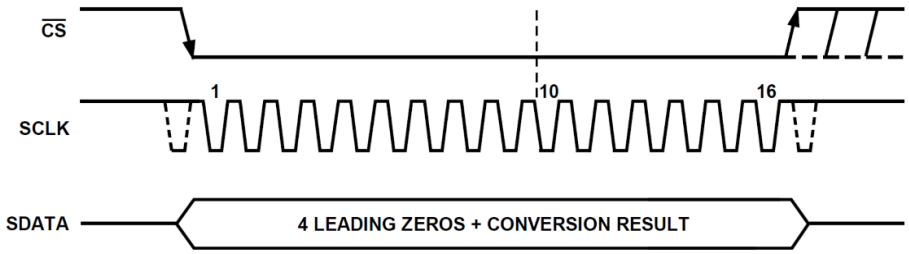
See the figure below for a typical connection circuit for the SLS7476. The power supply should come from a stable power supply device such as an LDO. The 1μF and 10nF coupling capacitors should be placed as close to the SLS7476 pins as possible. Always set the VDD power supply to be greater than or equal to the maximum VIN input signal to avoid maximum conversion code saturation.



Circuit connection diagram

4.Timing diagram

Normal mode timing. When the CS pin is low and the serial clock SCLK signal is provided, the SLS7476 can start a conversion cycle, as shown in the figure. The device outputs data during the conversion process, and the data is in MSB format, and the 12-bit converted data is output after 4 leading zeros. At the 16th falling edge of SCLK, SDATA enters the tri-state and the conversion cycle ends. CS is pulled high after 16 clock SCLKs until the time 1μS after SDATA enters the tri-state ends, and the next conversion can be started by pulling CS low again.



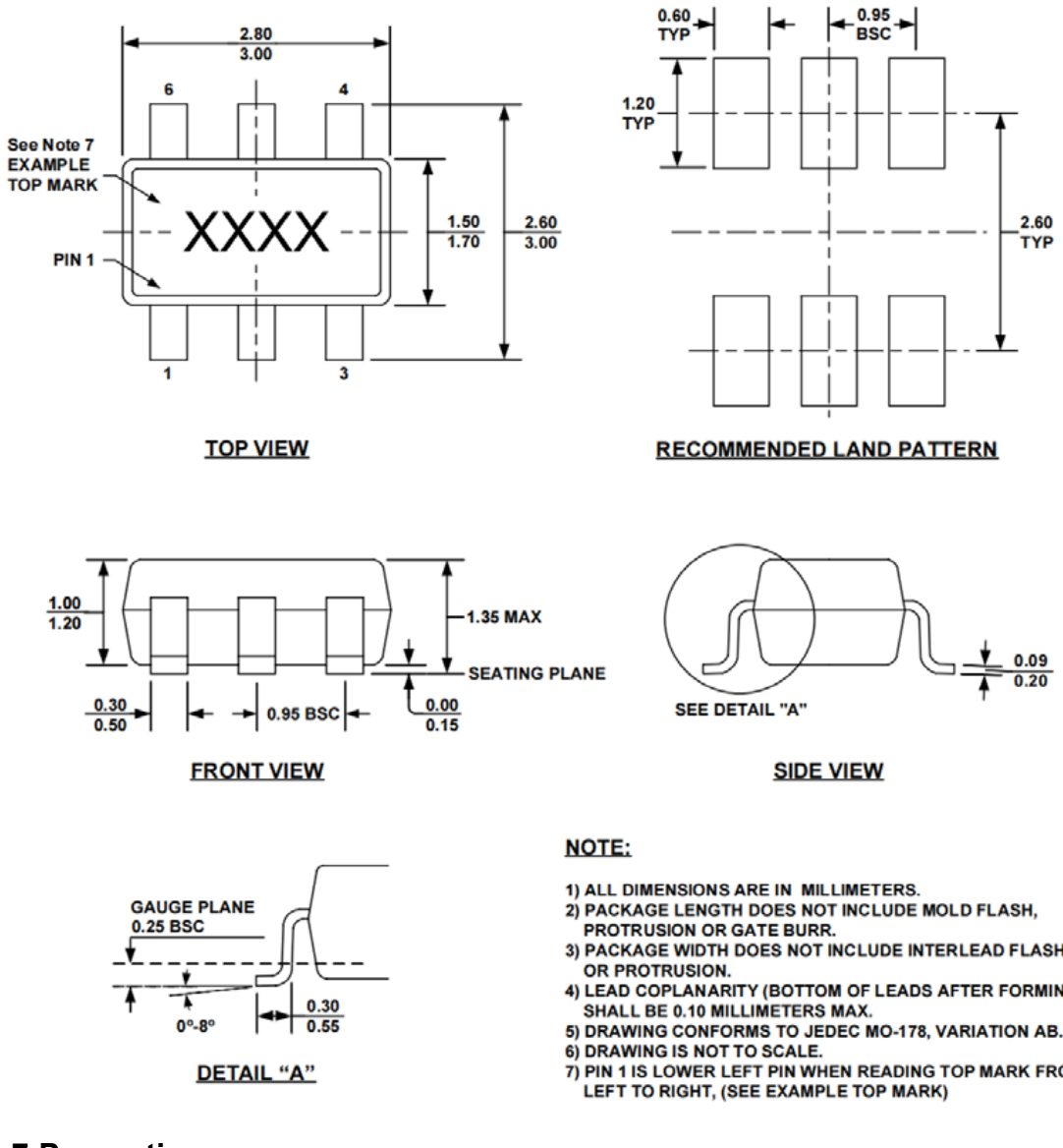
n=10

5.Conversion results

The SLS7476/77/78 series has an automatic power-down function. After shutting down all circuits, the converter usually consumes only a small current in this mode. When the CS falling edge appears, the device automatically wakes up. However, all functional blocks are fully enabled only when the third falling edge of SCLK appears. After the 16th falling edge of SCLK of the SLS7476, the device detects the end of the conversion and the device automatically powers down again. If CS is pulled high before 10 SCLKs, the SLS7476 will terminate the ongoing data conversion process, the converter will be forced into power-down mode, and there will be no valid data in the next conversion.

The higher the frequency of SCLK, the lower the power consumption of the converter at a fixed throughput rate, because the conversion time is shorter in a fixed period of time, that is, the converter is in automatic power-down mode more in each conversion cycle. For a specific SCLK frequency, the sampling time (CS falling edge to the third falling edge of SCLK) and the conversion time (four leading zeros plus 12 SCLK cycles) are fixed, so lower throughput (i.e., longer total conversion cycle) increases the proportion of time that is powered off, thereby reducing power consumption.

6.Packaging diagram



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

7.Precautions

1.Unpacked ICs and tube-packed ICs must be stored in a dry cabinet with a humidity of <20% R.H.
2.Components must be stored in anti-static packaging bags after storage and access.
3.Anti-static damage: The device is an electrostatic sensitive device. Adequate anti-static measures should be taken during transmission, assembly, and testing.
4.Users should conduct an appearance inspection before use. The bottom, sides, and surroundings of the circuit must be bright before welding. If oxidation occurs, the circuit can be treated by deoxidation means. After the treatment, the circuit must be welded within 12 hours.