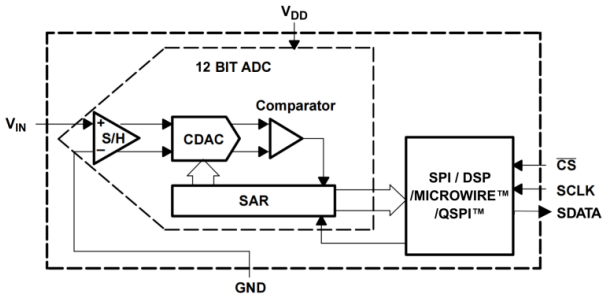
Features

- 1.5V-4.5V single power supply, automatic shutdown
- Ultra-low power consumption (typical)
  0.22mW (3.3V, 100KSPS)
  0.10mW (2.5V, 100KSPS)
  0.03mW (1.6V, 100KSPS)
- Maximum sampling rate 240 KSPS (1.5V-3.0V)
  Maximum sampling rate 1.2 MSPS (3.0V-4.5V)
- Maximum error ±0.5LSB INL, ±0.5LSB DNL
- 0-V_{DD} unipolar single-channel input
- SPI/DSP/MICROWIRE™/QSPI™ compatible serial interface schematic
- 6-pin SOT-23 package



Schematic

Packaging diagram

Application

- Battery powered systems
- Medical electronic equipment
- Standalone data acquisition equipment
- Remote data acquisition equipment

Description

1. The power supply voltage range is specified to be 1.5V-4.5V.
2. High speed and low power consumption. Up to 1.2 MSPS, the typical power consumption is 0.04mW at an operating voltage of 1.8V and 100KSPS.
3. Convenient power supply/serial clock speed management. The conversion rate is determined by the serial clock, and the conversion time can be reduced by increasing the serial clock speed. Automatic power-off after conversion can reduce the average power consumption when the power is off.

SL7467 is a 10-bit ADC (Analog-to-Digital Converter) chip, that is, an analog-to-digital converter, with the basic characteristics of ultra-low power consumption, small size, unipolarity, and single-ended input. SL7467 is designed with advanced process and technology, and has a wide voltage operating range:

When powered by a single power supply of 1.5V-3.0V, the sampling rate can reach up to 240 KSPS (compatible with similar chips);

When powered by a single power supply of 3.0V-4.5V, the sampling rate can reach up to 1.2 MSPS.

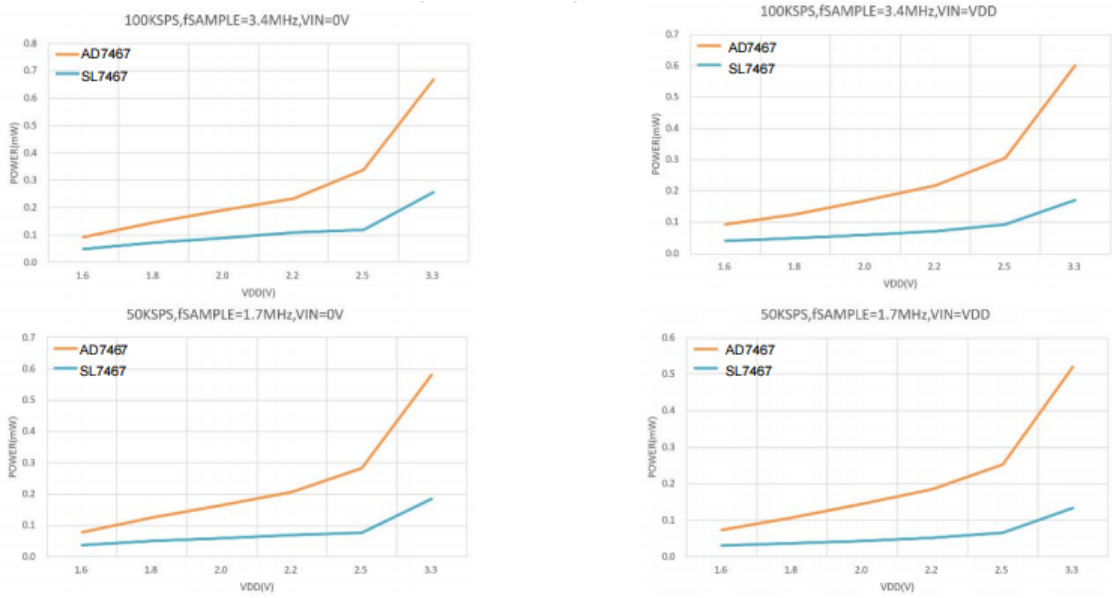
SL7467 adopts 6-pin SOT-23 package and has an operating temperature range of -40 to 85.

SL7467 can replace AD7467 pin-to-pin, and its dynamic power consumption is less than 1/2, which significantly extends the battery working time.

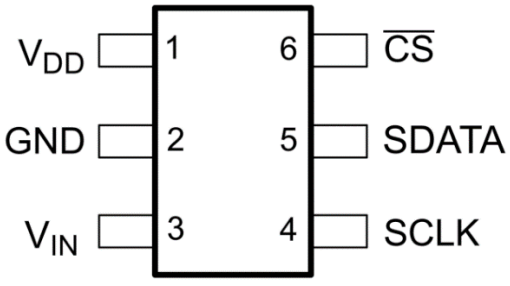
1.Main technical parameters

- 1.5V-4.5V single power supply
- 10-bit resolution, no missing codes
- Differential nonlinearity error (DNL): ±0.5 LSB
- Integral nonlinearity error (INL): ±0.5 LSB
- Signal-to-noise ratio distortion (SNR): 61 dB @30 KHz
- Total harmonic distortion (THD): -73 dB @30 KHz
- Unipolar single channel input, 0 V to V_{DD} range
- Maximum sampling rate 240 KSPS (1.5V-3.0V)
- Maximum sampling rate 1.2 MSPS (3.0V-4.5V)
- SPI/DSP/MICROWIRE™/QSPI™ compatible serial interface
- No pipeline cycle delay
- Automatic shutdown
- 6-pin SOT-23 package

Power comparison with AD7467(T=25℃):



2.Pin configuration

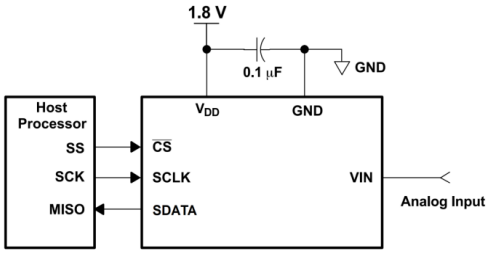


Pin diagram

Pin		Description
Name	Serial number	
V_{DD}	1	Power supply input. The V_{DD} range of the device is from 1.5V to 4.5V.
GND	2	Analog input signal ground. All analog and digital signals are referenced to this pin.
V_{IN}	3	Unipolar analog signal input. Input range is 0 to V_{DD}.
SCLK	4	Serial clock input. Clock is use to output data and source of the conversion clock.
SDATA	5	This is serial data output of the conversion result. The serial stream is MSB first.
CS	6	Chip select signal, active low, select SCLK, start conversions and frame out data.

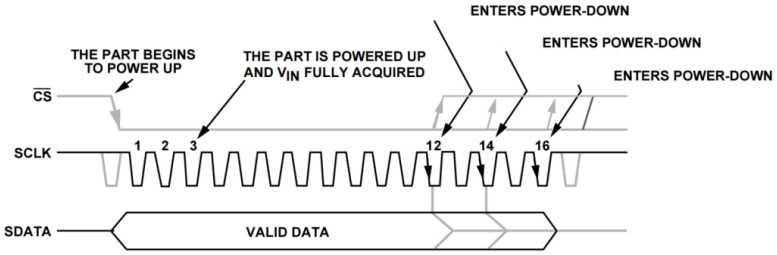
3.Typical connection

See the figure below for a typical connection circuit of the SL7467. The 1.8 V power supply should come from a stable power supply device such as an LDO.
A 0.1 μF coupling capacitor is required between the VDD pin and the GND pin of the SL7466 . The capacitor should be as close as possible to the pin of the SL7466.



Circuit connection diagram

4.Timing diagram



Timing diagram

A conversion cycle is initiated when the CS pin is pulled low and the serial clock SCLK signal is provided. After the CS falling edge, the time between the 3rd falling edge of SCLK (T sample) is used to sample the input signal. After the 3rd SCLK falling edge, the ADC enters the hold mode/conversion cycle (Tconvert) and begins the digitization process of the sampled input signal. At the 16th falling edge of SCLK, SDO enters the high impedance state and the conversion cycle ends.

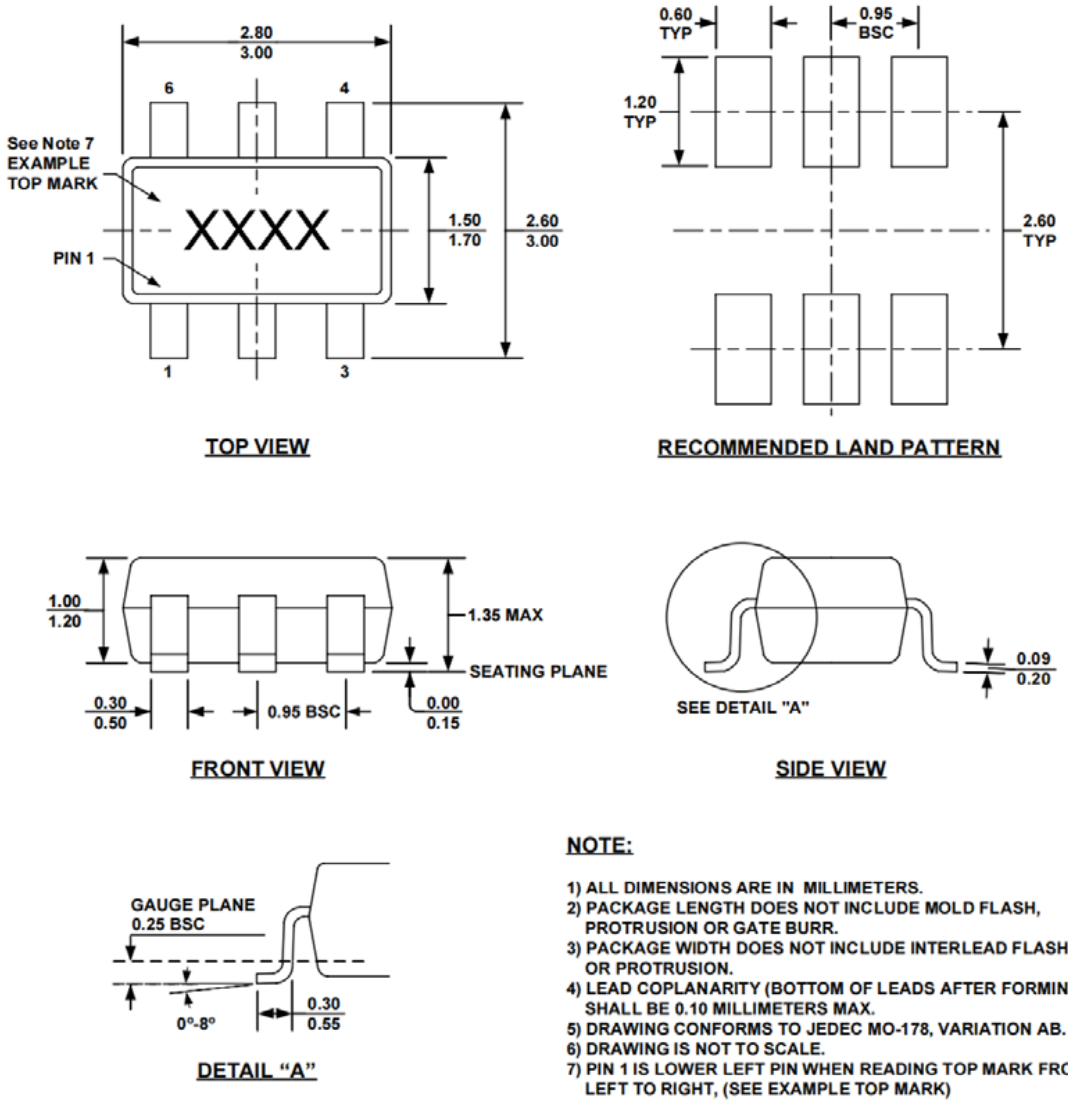
5.Conversion results

The SL7467 outputs 10 bits of converted data after 4 leading zeros, and these codes are in standard binary format.

Description	Analog input voltage	Digital output system	
		Binary	Hexadecimal
SL7467(10 bit)			
Least Significant Bit (LSB)	Vop/4096		
Full Scale	VDp-1LSB	11 1111 1111	3FF
Mid Scale	Vpp/2	10 0000 0000	200
Mid Scale-1LSB	Vpp/2-1LSB	01 1111 1111	1FF
Zero	0V	00 0000 0000	000

After power-up, the SL7467 has no specific initialization requirements, but the first conversion will not produce valid results. To set the SL7467 to a known state, CS is changed from low to high after VDD stabilizes during power-up. This puts the SL7467 in auto-shutdown mode, and the serial data output (SDO) is high impedance. The next time the CS pin is lowered and the serial clock SCLK signal is provided, the conversion can be performed normally and the result can be output.

6.Packaging diagram



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

7.Precautions

1.Unpacked ICs and tube-packed ICs must be stored in a dry cabinet with a humidity of <20% R.H.
2.Components must be stored in anti-static packaging bags after storage and access.
3.Anti-static damage: The device is an electrostatic sensitive device. Adequate anti-static measures should be taken during transmission, assembly, and testing.
4.Users should conduct an appearance inspection before use. The bottom, sides, and surroundings of the circuit must be bright before welding. If oxidation occurs, the circuit can be treated by deoxidation means. After the treatment, the circuit must be welded within 12 hours.