Ultra-low power 1000 KSPS 12-bit analog-to-digital converter (ADC)

Features

- 3.3V-5.25V Single Supply (SL2360/61/62)
  3.0V-4.8V single supply (SL2360E/61E/62E)
- Maximum sampling rate:
  100/250/500 KSPS (SL2360/61/62)
  Maximum sampling rate:
  1000 KSPS (SL2360E/61E/62E)
- Ultra-low power consumption (SL 2360 typical)
  0.60mW (3.3V, 100KSPS)
  0.80mW (4V, 100KSPS)
- Automatic shutdown
- Tolerance ±0.5LSB INL, ±0.5LSB DNL
- 0-VDD unipolar single channel input
- SPI/MICROWIRE™ compatible serial interface
- 6-pin SOT-23 package
- Operating temperature range from -40°C to 85°C

Application

- Communication system
- Data acquisition systems
- Handheld Portable Devices
- Uninterruptible Power Supply Equipment
- Battery powered systems
- In-vehicle electronics

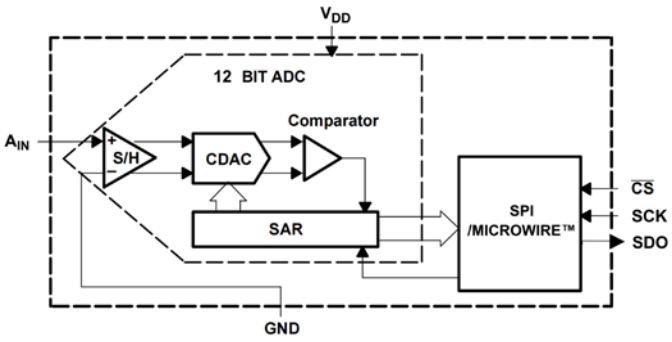
Description

The SL2360 / SL2361 / SL2362 series are 12-bit sampling A/D converters. The supply current decreases as the sampling rate drops because these devices automatically power down after the conversion is completed. The input signal range for conversion is from 0V to VDD. They feature ultra-low power consumption, small size, unipolar operation, and single-ended inputs. The product is available in two versions:

The SL2360/SL2361/SL2362 versions operate with a single supply voltage ranging from 3.3V to 5.25V, and support sampling rates of up to 100/250/500 KSPS.

The SL2360E/SL2361E/SL2362E versions operate with a single supply voltage ranging from 3.0V to 4.8V, and support sampling rates of up to 1000 KSPS.

Both versions feature a 6-pin SOT-23 package and operate within a temperature range of -40°C to 85°C.The SL2360/SL2361/SL2362 can be pin-to-pin replacements for the LTC2360/LTC2361/LTC2362, with dynamic power consumption less than half of theirs, significantly extending battery life.



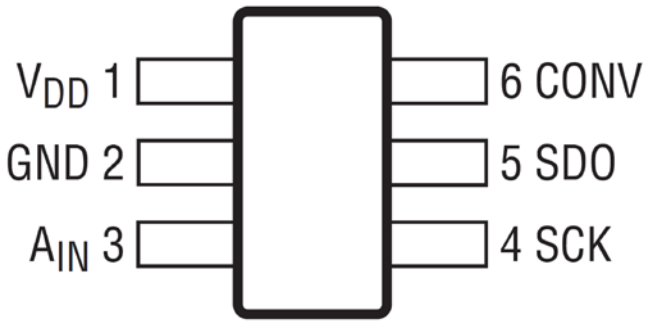
Schematic

Package schematic

1.Main technical parameters

- 3.3V-5.25V Single Supply (SL2360/61/62)
  3.0V-4.8V single supply (SL2360E/61E/62E)
- Maximum sampling rate:100/250/500 KSPS (SL2360/61/62)
  Maximum sampling rate:1000 KSPS (SL2360E/61E/62E)
- 12-bit resolution, no missing codes
- Differential non-linearity error (DNL): ±0.5 LSB
- Integral nonlinearity error (INL): ±0.5 LSB
- Signal-to-Noise Distortion (SNR): 72.4 dB @100 KHz
- Total Harmonic Distortion (THD): -84 dB @100 KHz
- SPI/MICROWIRE™ compatible serial interface
- Auto shutdown
- Ultra-low power consumption (typical)
  SL 2360
  0.60mW (3.3V, 100KSPS)
  0.80mW (4.0V, 100KSPS)
  SL 2361
  1.15mW (3.3V, 250KSPS)
  1.65mW (4.0V, 250KSPS)
  SL 2362
  1.68mW (3.3V, 500KSPS)
  2.50mW (4.0V, 500KSPS)
- No pipeline cycle delay
- Unipolar single-channel input, 0 V to VDD range
- 6-pin SOT-23 package

2.Pin

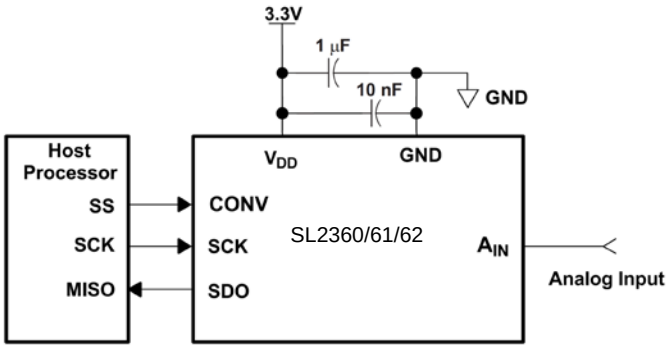


Pin-out diagram

Pinout		Descriptions
Name	Serial number	
V_{DD}	1	Power input.
GND	2	The analog input signal is grounded. All analog and digital signals are referenced to this pin.
A_{IN}	3	Unipolar analog signal input. Input range is 0 to V_{DD}.
SCK	4	Serial clock input. sck Serial clock synchronization Serial data transfer.
SDO	5	Serial data output of the conversion result. The serial stream is MSB prioritized.
CONV	6	Chip Select Signal. Active low is used to select the SCK input, initiate conversions, and frame the output data.

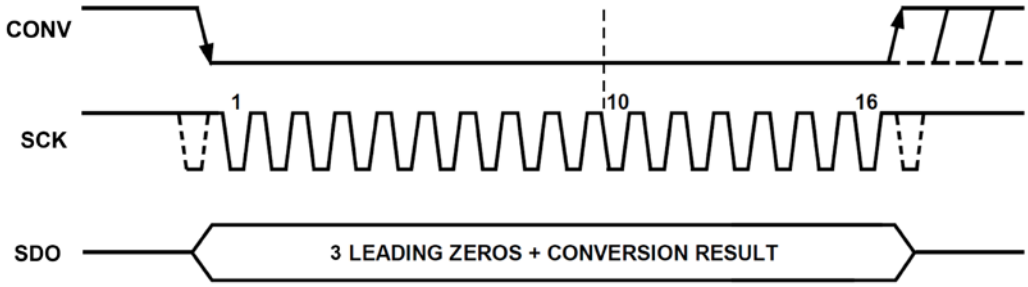
3.Typical connections

Typical connection circuits for the SL 2360/61/62 series are shown in the figure below.
The power supply should come from a stabilized power supply device such as an LDO. a 1 μF and a 10 nF coupling capacitor is required between the VDD pin and the GND pin of the SL 2360/61/62. This capacitor should be as close as possible to the pins of the SL 2360/61/62 series.



Wiring diagram

4.Sequence diagram



Sequence diagram

The LTC2360/LTC2361/LTC2362 immediately outputs the conversion result through SDO after the falling edge of CONV, whereas the SL2360/SL2361/SL2362 outputs the 12-bit conversion result from SDO after the fourth falling edge of SCK following the CONV falling edge. After that, SDO enters a high-impedance state, marking the end of the conversion cycle. The higher the SCK frequency, the lower the power consumption of the converter at a fixed throughput rate, as the conversion time is shorter within the fixed time period, meaning the converter spends more time in automatic shutdown mode during each conversion cycle.

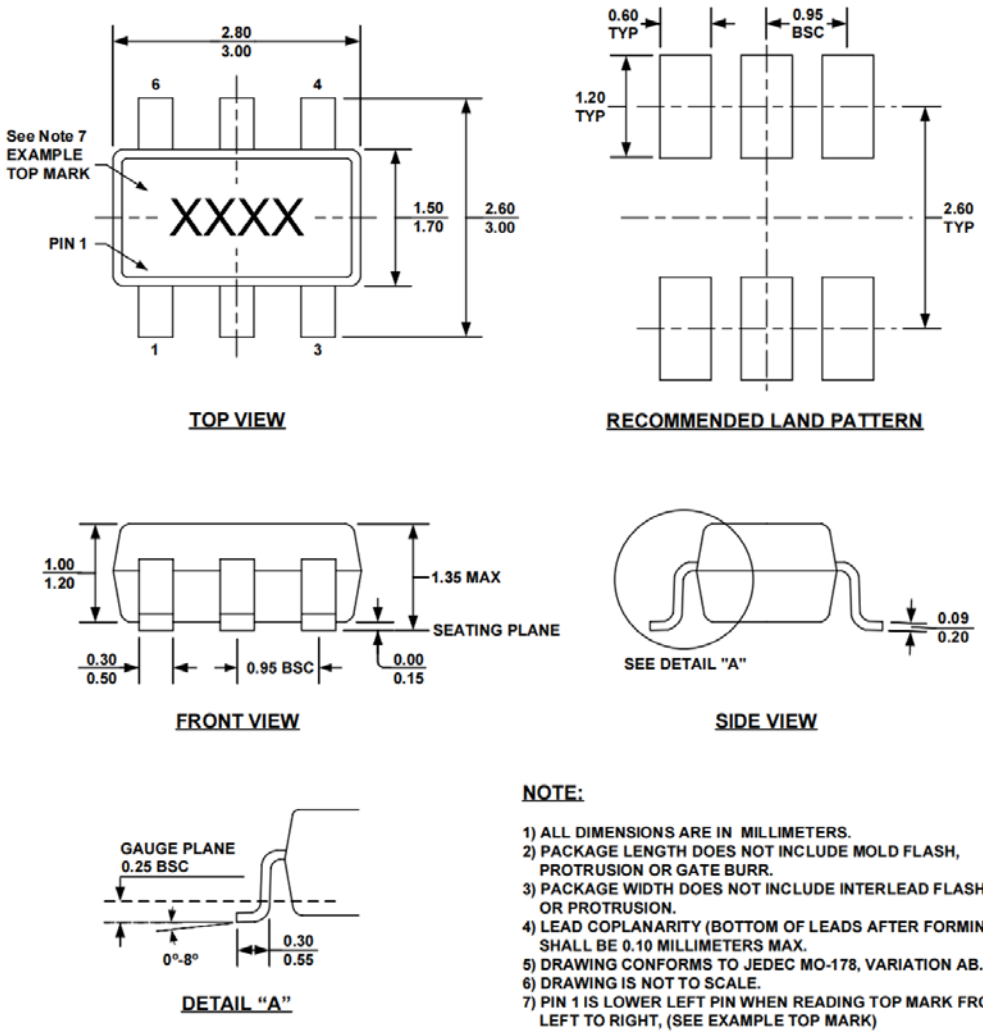
5.Conversion results

The SL 2360/SL2361/SL2362 output 12-bit converted data, and these codes are in standard binary format.

Description	Analog input voltage	Digital output binary	
		Binary system	Hexadecimal
SL2360/SL2361/SL2362 （12 位）			
Least Significant Bit (LSB)	V_{DD}/4096		
Full Scale	V_{DD} – 1LSB	1111 1111 1111	FFF
Mid Scale	V_{DD}/2	1000 0000 0000	800
Mid Scale – 1LSB	V_{DD}/2 – 1LSB	0111 1111 1111	7FF
Zero	0V	0000 0000 0000	000

After power-up, the SL2360/61/62 has no specific initialization requirements, but the first conversion will not produce valid results. To set the SL2360/61/62 to a known state, after VDD stabilizes during power-up, the CONV pin should be driven from low to high. This places the SL2360/61/62 into automatic shutdown mode, and the serial data output (SDO) will be in a high-impedance state. The next time the CONV pin is driven low and the serial clock (SCK) signal is provided, the converter will perform a normal conversion and output the result.

6.Package schematic



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

7.Precautions

1.Unpacked ICs, ICs in tubes, etc. must be stored in a dry cabinet with humidity <20% R.H.

2.After accessing the components are stored in electrostatic packaging protective bags.

3.Anti-static damage: the device is electrostatic sensitive devices, transmission, assembly, testing process should take adequate anti-static measures.

4.users should be used before the appearance of the inspection, the circuit bottom, sides, around the bright before welding. If there is oxidation can be taken to oxidize the means to deal with the circuit, the circuit must be completed within 12 hours to complete the welding process.