8/10/12-bit ultra-low power 1MSPS analog-to-digital converter (ADC)

Description

The SL11661/SL11663/SL11665 series are analog-to-digital converters (ADC) with basic features including 8/10/12-bit resolution, ultra-low power consumption, small size, unipolar, and single-ended input. They offer convenient power/ serial clock speed management. The conversion rate is determined by the serial clock, and conversion time can be reduced by increasing the serial clock speed. With the ability to automatically shut down, the automatic power-down after conversion helps reduce average power consumption. This series is available in two versions:

The SL11661/63/65 versions are powered by a single 3.3 V to 5.25 V supply and offer sample rates up to 500 KSPS.

The SL11661 A/63A/65A versions are powered by a single 3.0 V-4.5 V supply with sample rates up to 1 MSPS.

The SL 11661/SL11663/SL11665 series are all available in a 6-pin SOT-23 package with an operating temperature range of -40°C to 85°C.

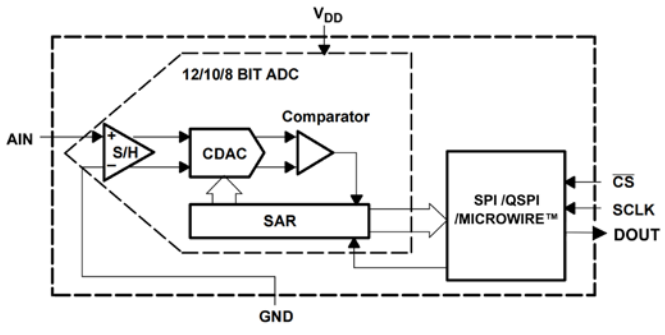
The SL11661/SL11663/SL11665 are pin-to-pin replacements for the MAX11661/MAX11663/ MAX11665 and consume less than 1/2 the dynamic power, significantly extending battery life.

Feature

- 3.0V-4.5V single power supply (SL11661A/63A/65A)
  3.3V-5.25V single supply (SL11661/63/65)
- Maximum sampling rate 1 MSPS (SL11661A/63A/65A)
- Maximum sampling rate 500 KSPS (SL11661/63/65)
- Automatic shutdown
- Ultra-low power consumption (12bit typical)
  1.6mW (3.3 V, 500KSPS)
  2.4mW (4 V, 500KSPS)
- Tolerance ±0.5LSB INL, ±0.5LSB DNL
- 0-V_{DD} unipolar single channel input
- SPI/QSPI/MICROWIRE™ Compatible Serial Interface
- 6-pin SOT-23 package
- Operating temperature range from -40°C to 85°C

Application

- Communication systems
- Data acquisition system
- Handheld portable devices
- Medical instruments
- Battery powered systems
- In-vehicle electronics



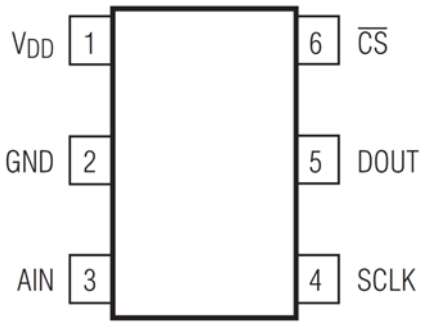
Schematic

Package schematic

1.Main technical parameters

- ●3.0V-4.5V Single Supply (SL11661A/63A/65A)
  3.3V-5.25V single supply (SL11661/63/65)
- ●Ultra-low power consumption (typical)
  SL11661 (8 bit)
  1.4mW (3.3V, 500KSPS)
  2.2mW (4V, 500KSPS)
  SL 11663 (10 bit)
  1.5mW (3.3V, 500KSPS)
  2.3mW (4V, 500KSPS)
  SL 11665 (12bit)
  1.6mW (3.3V, 500KSPS)
  2.4mW (4V, 500KSPS)
- ●Maximum Sample Rate 1 MSPS (SL11661A/63A/65A)
- ●Maximum sampling rate 500 KSPS (SL11661/63/65)
- ●8/10/12-bit resolution, no missing codes
- ●Differential non-linearity error (DNL): ±0.5 LSB
- ●Integral nonlinearity error (INL): ±0.5 LSB
- ●Signal-to-Noise Distortion (SNR): 72 dB @100 KHz
- ●Total Harmonic Distortion (THD): -83 dB @100 KHz
- ●SPI/QSPI/MICROWIRE™ compatible serial interface
- ●No pipeline cycle delay
- ●Auto shutdown
- ●Unipolar single-channel input, 0 V to VDD range
- ●6-pin SOT-23 package

2.Pin

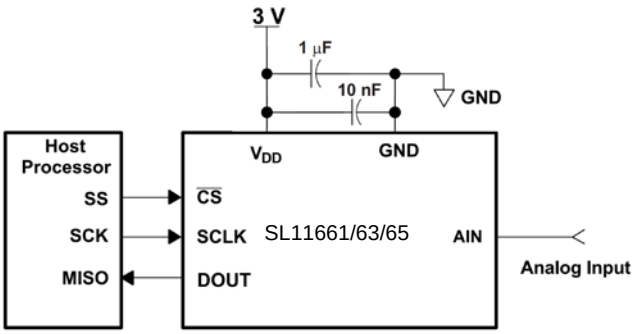


Pinout

Pinout		Description
Name	Serial number	
V_{DD}	1	Power input. Also similar to the reference voltage of an ADC.
GND	2	The analog input signal is grounded. All analog and digital signals are referenced to this pin.
AIN	3	Unipolar analog signal input. Input range is 0 to V_{DD}.
SCLK	4	Serial Clock Input. This clock is used to output data and is also the source of the conversion clock.
DOUT	5	This is the serial data output of the conversion result. The serial stream has MSB priority.
$\overline{CS}$	6	The chip select signal, active low, is used to select on the SCLK input, initiate conversions, and frame the output data.

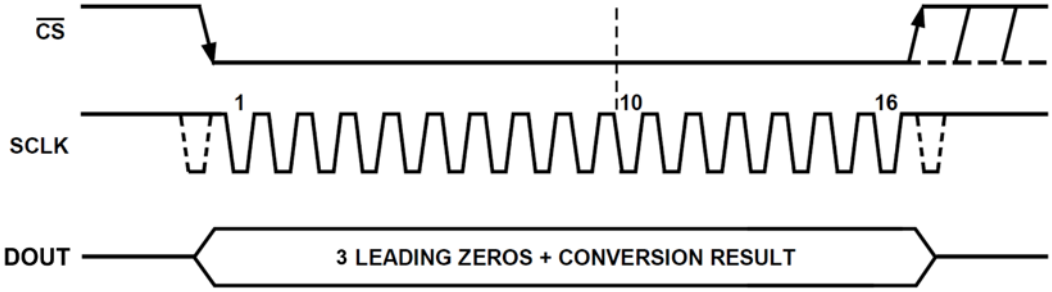
3.Typical connections

The typical connection diagram for the SL11661/63/65 series is shown below. The power supply should come from a stable source, such as an LDO. A 1 μF and a 10 nF coupling capacitor are required between the VDD and GND pins of the SL11661/63/65 series. The capacitors should be placed as close as possible to the pins of the SL11661/63/65 series.



Circuit connection diagram

4.Sequence diagram



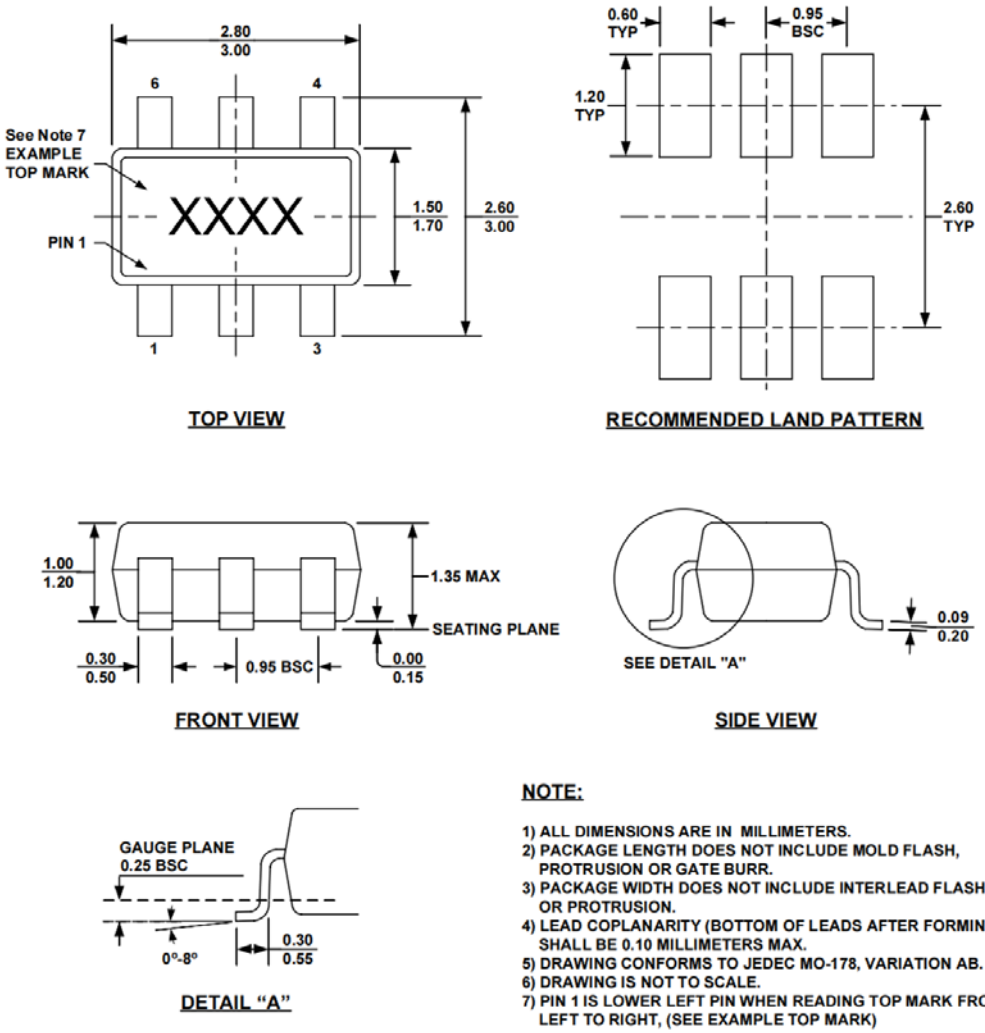
Chronology

Unlike the MAX11661/63/65 series, which outputs the conversion result through DOUT after the second falling edge of SCLK following the CS falling edge, the SL11661/63/65 series outputs three leading zeros followed by the 8/10/12-bit conversion result from DOUT after the fourth falling edge of SCLK following the CS falling edge. For the 8-bit result, four trailing zeros follow; for the 10-bit result, two trailing zeros follow. Afterward, DOUT enters a high-impedance state, signaling the end of the conversion cycle.

5.Battery saving mode

The SL11661/63/65 series features an automatic power-down function. After all circuits are turned off, the converter typically consumes very little current in this mode. When the CS line goes low, the device automatically wakes up. However, all functional blocks are fully powered on only after the third falling edge of SCLK. Once the 12th/14th/16th falling edge of SCLK occurs, the device detects the completion of the conversion and automatically enters power-down mode again.If the CS line is pulled high before the 10th falling edge of SCLK, the SL11661/63/65 will abort the ongoing data conversion process, forcing the converter into power-down mode, and no valid data will be available for the next conversion. The higher the SCLK frequency, the lower the converter's power consumption at a fixed throughput, as the conversion time is shorter within a fixed time period. This means the converter spends more time in automatic power-down mode during each conversion cycle. For a specific SCLK frequency, the sampling time (from the CS falling edge to the third falling edge of SCLK) and conversion time (three leading zeros followed by 10 SCLK cycles) are fixed. Therefore, at lower throughput (i.e., when the total conversion cycle is longer), the proportion of time spent in power-down mode increases, resulting in reduced power consumption.

6.Package schematic



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

7.Precautions

1. Unpacked ICs, ICs in tubes, etc. must be stored in a dry cabinet with humidity <20% R.H. 2.

2. After storage, the components are stored in electrostatic packaging protective bags.

3. Anti-static damage: the devices are electrostatic sensitive devices, adequate anti-static measures should be taken during transmission, assembly and testing.

4. Users should carry out an appearance check before use, the circuit bottom, sides, around the bright before welding. If there is oxidation

Oxidation can be taken to oxidize the means of treatment of the circuit, the completion of the circuit must be completed within 12 hours of welding.