12-bit Ultra-Low Power Single Channel 3.3 V - 5.25 V Operating Voltage 1000 KSPS Analog-to-Digital Converter (ADC)

Feature

- 4 V - 5.25 V single supply (SL2365)
  3.3 V - 4.8 V single supply (SL2365E)
- Ultra-low power consumption (typical)
  3.40mW (4V, 800 KSPS)
  5.95mW (5V, 800 KSPS)
- SL2365 Maximum Sample Rate: 800 KSPS
  SL2365E Maximum Sample Rate: 1000 KSPS
- Tolerance ±0.5LSB INL, ±0.5LSB DNL
- 0-VDD Unipolar single channel input
- SPI/MICROWIRE™ compatible serial interface
- 6-pin SOT-23 package
- Operating temperature range from -40°C to 85°C

Application

- Communication Systems
- Data Acquisition System
- Handheld portable equipment
- Uninterruptible power supply equipment
- Battery powered systems
- In-vehicle electronics

Description

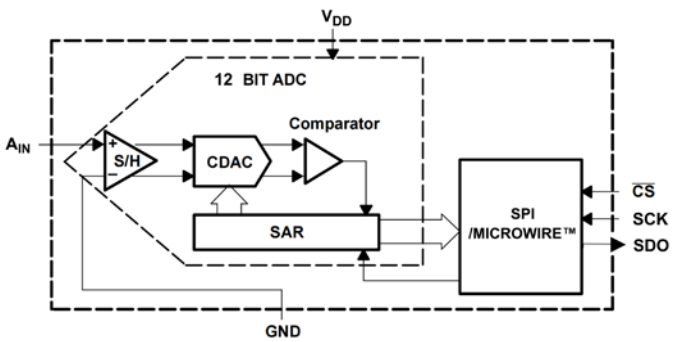
The SL2365 is a 12-bit ADC (Analog-to-Digital Converter) chip. Because these devices automatically power down after the conversion is complete, the supply current drops as the sampling rate decreases.The SL2365 converts signals over an input range of 0V to VDD. with the basic features of ultra-low power consumption, small size, unipolar, and single-ended input. The product is available in two versions:

The SL2365 version is powered by a single 4V-5.25V supply and has a sampling rate of up to 800KSPS.

The SL2365E version is powered by a single 3.3V-4.8V supply and has a sampling rate of up to 1000KSPS.

Both versions are available in a 6-pin SOT-23 package with an operating temperature range of -40°C to 85°C. The SL2365E version is available in a single 3.3V-4.8V power supply with sample rates up to 1000KSPS.

The SL2365 is a pin-to-pin replacement for the LTC2365 and consumes less than 1/3 of the dynamic power, significantly extending battery life.



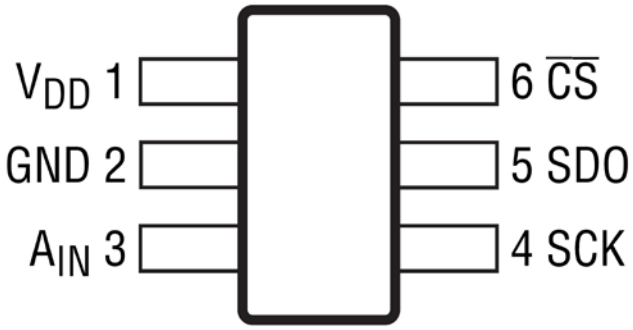
Schematic

Package schematic

1.Main technical parameters

- ●4 V - 5.25 V single supply (SL2365)
  3.3 V - 4.8 V single supply (SL2365E)
- ●4 V - 5.25 V single supply (SL2365)
  3.3 V - 4.8 V single supply (SL2365E)
- ●Differential nonlinearity error (DNL): ±0.5 LSB
- ●Integral nonlinearity error (INL): ±0.5 LSB
- ●Ultra-low power consumption (typical)
  SL 2365
  3.40mW (4V, 800 KSPS)
  5.95mW (5V, 800 KSPS)
- ●SL2365 Maximum Sample Rate: 800 KSPS
  SL2365E Maximum sample rate: 1000 KSPS
- ●Signal-to-Noise Distortion (SNR): 72.5 dB @ 100 KHz
- ●Total Harmonic Distortion (THD): -85 dB @100 KHz
- ●SPI/MICROWIRE™ compatible serial interface
- ●No pipeline cycle delay
- ●Auto shutdown
- ●Unipolar single-channel input, 0 V to VDD range
- ●6-pin SOT-23 package

2.Pin

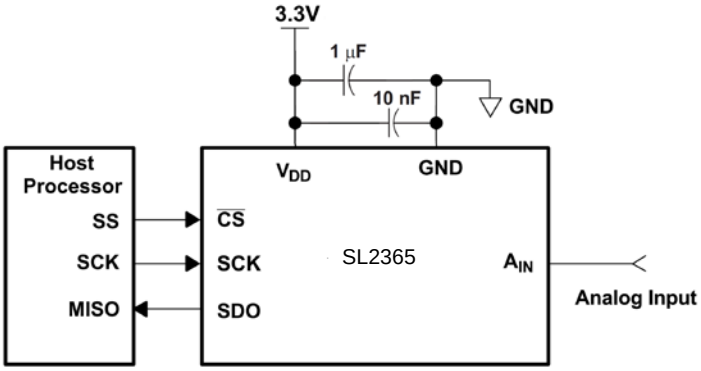


Pinout

Pinout		Description
Name	serial number	
V_{DD}	1	Power input.
GND	2	The analog input signal is grounded. All analog and digital signals are referenced to this pin.
A_{IN}	3	Unipolar analog signal input. Input range is 0 to VDD.
SCK	4	Serial clock input. sck Serial clock synchronization Serial data transfer.
SDO	5	Serial data output of the conversion result. The serial stream is MSB prioritized.
$\overline{CS}$	6	Chip Select Signal. Active low is used to select the SCK input, initiate conversions, and frame the output data.

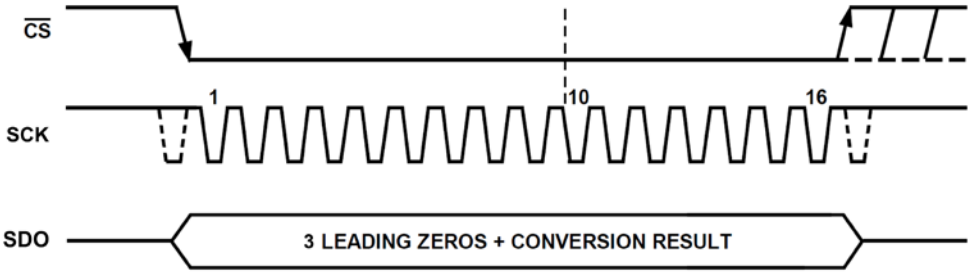
3.Typical connections

The typical connection circuit for the SL2365 is shown in the diagram below. The power supply should come from a stable power source, such as an LDO. A 1 μF and a 10 nF decoupling capacitor are required between the VDD and GND pins of the SL2365. These capacitors should be placed as close as possible to the SL2365 pins.



Circuit connection diagram

4.Sequence diagram



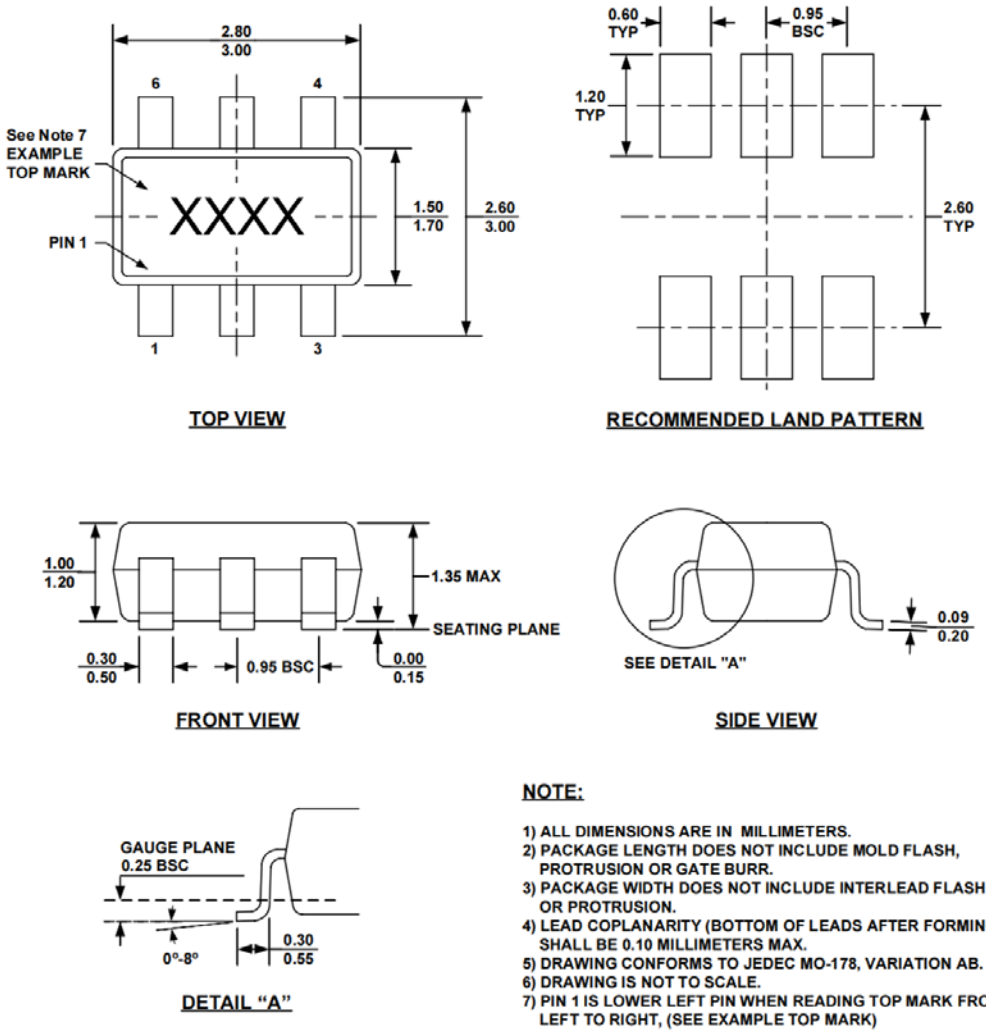
Chronology

The LTC2365 outputs the conversion result via SDO after the second falling edge of SCK following the falling edge of CS. In contrast, the SL2365 series outputs three leading zeros followed by the 12-bit conversion result from SDO after the fourth falling edge of SCK following the falling edge of CS. After this, SDO enters a high-impedance state, and the conversion cycle is complete.

5.Battery saving mode

The SL2365 features an automatic power-down function. Once all circuits are powered off, the converter typically consumes very little current in this mode. When a falling edge of CS occurs, the device automatically wakes up. However, all functional blocks are fully activated only after the third falling edge of SCK. After the 16th falling edge of SCK, the device detects the end of the conversion and automatically powers down again. If CS is pulled high before 10 SCLKs have passed, the SL2365 will abort the ongoing data conversion process, forcing the converter into power-down mode, and no valid data will be available for the next conversion. The higher the SCK frequency, the lower the power consumption of the converter at a fixed throughput rate, because the conversion time is shorter within a fixed time period, meaning the converter spends more time in automatic power-down mode during each conversion cycle. For a specific SCK rate, the sampling time (from the falling edge of CS to the third falling edge of SCK) and conversion time (three leading zeros plus 10 SCK cycles) are fixed. Therefore, at lower throughput (i.e., when the overall conversion cycle is extended), the proportion of time spent in power-down mode increases, resulting in reduced power consumption.

6.Package schematic



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

7.Precautions

1. Unpacked ICs, ICs in tubes, etc. must be stored in a dry cabinet with humidity <20% R.H. 2.

2. After storage, the components are stored in electrostatic packaging protective bags.

3. Anti-static damage: the devices are electrostatic sensitive devices, adequate anti-static measures should be taken during transmission, assembly and testing.

4. Users should carry out an appearance check before use, the circuit bottom, sides, around the bright before welding. If there is oxidation

Oxidation can be taken to oxidize the means of treatment of the circuit, the completion of the circuit must be completed within 12 hours of welding.