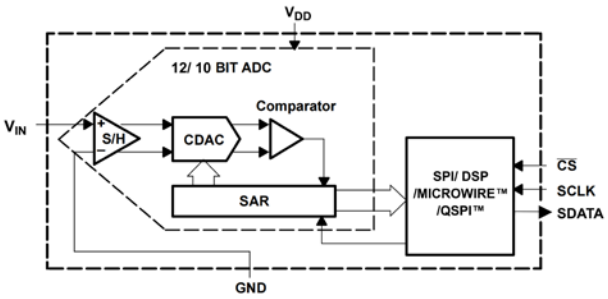
Ultra-low power consumption 3.3V-5.25V operating voltage 250KSPS 10/12-bit analog-to-digital converter (ADC)

Feature

- 3.3V-5.25V single supply with auto power off
- Ultra-low power consumption (12-bit typical)
  1.1mW (3.3V, 250KSPS)
  2.8mW (5V, 250KSPS)
- Maximum Sample Rate 250 KSPS
- Error ±0.5LSB INL, ±0.5LSB DNL
- Signal-to-Noise Distortion (SNR): 71.5 dB @100 KHz
- 0-VDD unipolar single-channel inputs
- SPI/DSP/MICROWIRE™/QSPI™ compatible serial interface
- 6-pin SOT-23 package (stock)
- 6-pin SC-70 and 8-pin MSOP packages (program)



Schematic

Application

- Battery Powered Systems
  Personal Digital Devices
  Medical Instruments
  Mobile communications
- Instrumentation and control systems
- Data acquisition systems
- High-speed modems
- Optical sensors

Packaging effect diagram

Product highlights

- No pipeline cycle delay.
- Ultra-low power consumption. Up to 250KSPS, 12bit at 5V, 250KSPS typical power consumption of 2. 8mW. 3.
- Convenient power supply/serial clock speed management. The conversion rate is determined by the serial clock, and the conversion time can be reduced by increasing the serial clock speed.

The conversion rate is determined by the serial clock, and the conversion time can be reduced by increasing the serial clock speed. Automatic power-down after conversion reduces average power consumption during power-down.

The SL7910/SL7920 are 10/12-bit ADC (Analog-to-Digital Converter) chips, featuring ultra-low power consumption, compact size, unipolar, single-ended inputs. These products operate with a single supply voltage ranging from 3.3V to 5.25V, with a maximum sampling rate of 250KSPS. They come in a 6-pin SOT-23 package and have an operating temperature range of -40°C to 85°C.

The SL7910/SL7920 can be pin-to-pin replacements for the AD7910/AD7920, while consuming less than one-third of their dynamic power, significantly extending battery life.

1.Main technical parameters

- ●3.3V-5.25V single power supply
- ●Maximum sampling rate 250 KSPS
- ●Ultra-low power consumption (typical)

  SL7910

  0.9mW (3.3V, 250KSPS)

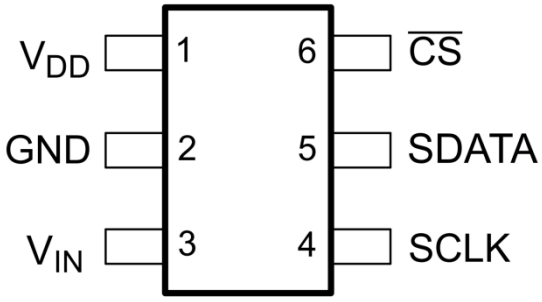
  2.5mW (5V, 250KSPS)

  SL7920

  1.1mW (3.3V, 250KSPS)

  2.8mW (5V, 250KSPS)
- ●10/12-bit resolution, no missing codes
- ●Differential Nonlinearity Error (DNL): ±0.5 LSB
- ●Integral Nonlinearity Error (INL): ±0.5 LSB
- ●Signal-to-Noise Distortion (SNR): 71.5 dB @100 KHz
- ●Total Harmonic Distortion (THD): -81 dB @100 KHz
- ●SPI/DSP/MICROWIRE™/QSPI™ compatible serial interface
- ●No pipeline cycle delay
- ●Auto shutdown
- ●Unipolar single-channel input, 0 V to V_{DD} range
- ●6-pin SOT-23 package

2.Pin

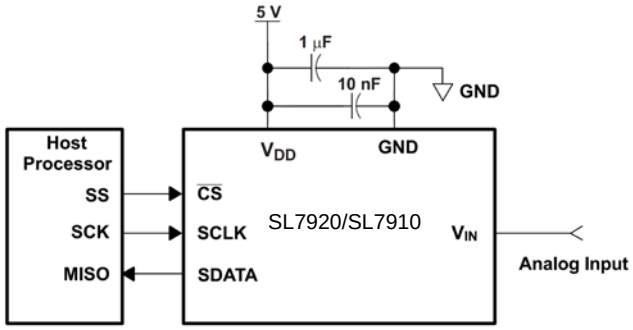


Pinout

Pinout		Description
Name	Serial number	
V_{DD}	1	Power input. The V_{DD} range for this device is from 3.3V to 5.25V.
GND	2	The analog input signal is grounded. All analog and digital signals are referenced to this pin.
V_{IN}	3	Unipolar analog signal input. Input range is 0 to V_{DD}.
SCLK	4	Serial Clock Input. This clock is used to output data and is also the source of the conversion clock.
SDATA	5	This is the serial data output of the conversion result. The serial stream has MSB priority.
$\overline{CS}$	6	The chip select signal, active low, is used to select on the SCLK input, initiate conversions, and frame the output data.

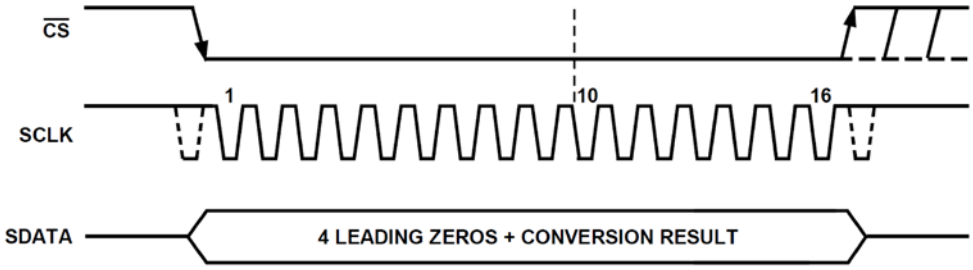
3.Typical connections

The typical connection diagram for the SL7910/SL7920 is shown below. The power supply should come from a stable source, such as an LDO. The 1 μF and 10nF coupling capacitors should be placed as close as possible to the pins. Always ensure that the VDD supply is greater than or equal to the maximum VIN input signal to avoid saturation of the maximum conversion code.



Circuit connection diagram

4.Sequence diagram



Chronology

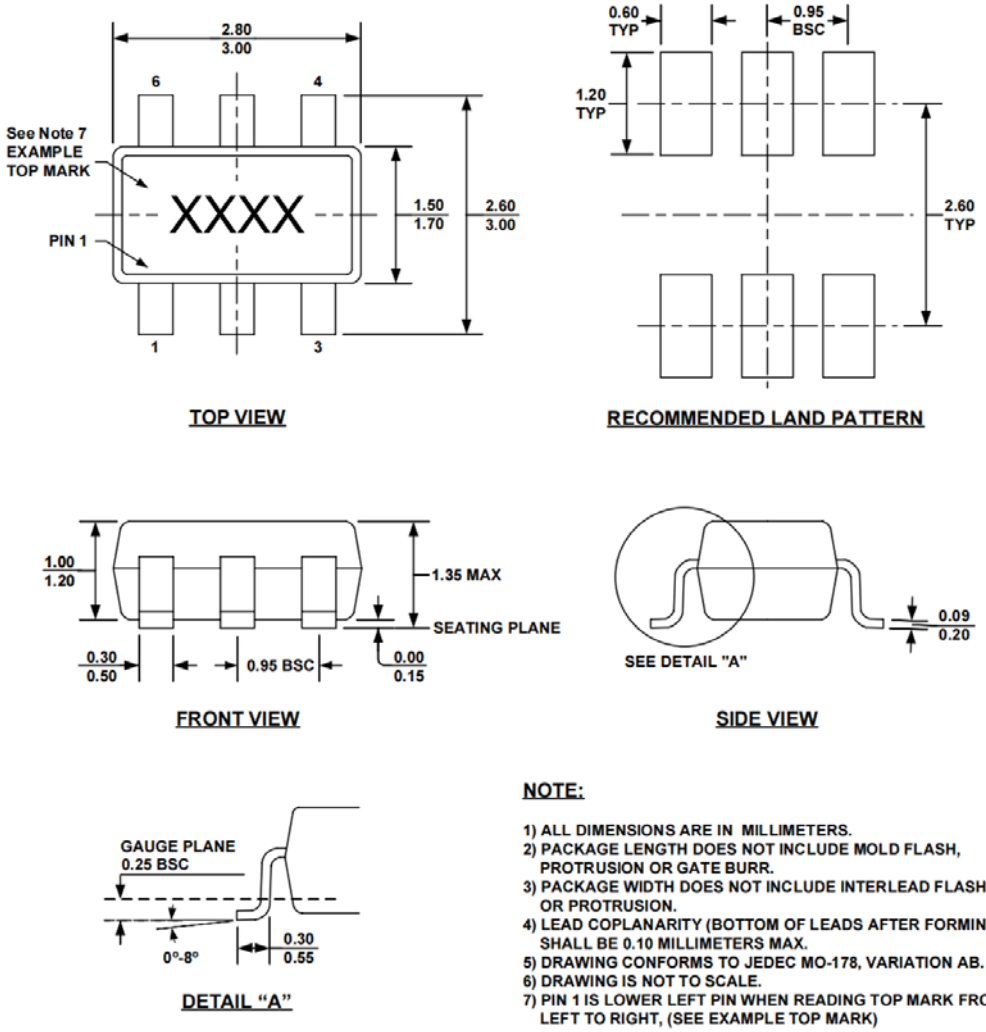
Normal mode timing: When the CS pin is pulled low and a serial clock (SCLK) signal is provided, the SL7910/SL7920 starts a conversion cycle as shown in the diagram. During the conversion, the device outputs data in MSB format. The SL7920 outputs 12-bit converted data after four leading zeros, while the SL7910 outputs 10-bit converted data after four leading zeros, followed by two trailing zeros. At the 16th falling edge of SCLK, the SDATA line enters high-impedance state, indicating the end of the conversion cycle. The CS pin is pulled high after 16 SCLK clock cycles, and after 1µs from the SDATA entering the high-impedance state, the CS pin can be pulled low again to begin the next conversion.

5.Battery saving mode

The SL7910/SL7920 series features an automatic power-down function. After all circuits are powered off, the converter typically consumes very little current in this mode. The device automatically wakes up when the CS pin is pulled low. However, all functional blocks are fully activated only after the third falling edge of the SCLK signal. After the 14th/16th falling edge of the SCLK signal, the device detects the end of the conversion and automatically powers down again. If the CS pin is pulled high before the 10th falling edge of the SCLK, the SL7910/SL7920 will abort the ongoing data conversion process, forcing the converter into power-down mode, and no valid data will be available during the next conversion.

As the SCLK frequency increases, the power consumption of the converter decreases at a fixed throughput rate because the conversion time becomes shorter within a fixed time period. This means the converter spends more time in the automatic power-down mode during each conversion cycle. For a specific SCLK frequency, the sampling time (from the falling edge of CS to the third falling edge of SCLK) and the conversion time (which includes four leading zeros and 12 SCLK cycles) are fixed. Therefore, when the throughput is lower (i.e., the total conversion cycle is longer), the proportion of time spent in power-down mode increases, resulting in a reduction in overall power consumption.

6.Package schematic



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

7.Precautions

- Unpacked ICs, ICs in tubes, etc. must be stored in a dry cabinet with humidity <20% R.H. 2.
- After storage, the components are stored in electrostatic packaging protective bags.
- Anti-static damage: the devices are electrostatic sensitive devices, adequate anti-static measures should be taken during transmission, assembly and testing.
- Users should carry out an appearance check before use, the circuit bottom, sides, around the bright before welding. If there is oxidation

  Oxidation can be taken to oxidize the means of treatment of the circuit, the completion of the circuit must be completed within 12 hours of welding.