Serial I²C bus EEPROM

Description

- The SL 24C02/04/08/16/32/64 series are electrically erasable PROM, featuring organizational structures of 256/512/1024/2048/4096/8192 × 8-bit, respectively, and utilize a two-wire serial interface (I²C). They support voltages as low as 1.8V, with standby current and operating current of 1μA and 1mA, respectively.

- The SL 24C02/04/08/16/32/64 series feature page write capability, with each page consisting of 8/16/16/16/32/32 bytes, respectively. They are available in three package types: 8-pin PDIP, 8-pin SOP, and 5-pin SOT-23-5.

Feature

- Wide operating voltage range of 1.8V to 5.5V.
- Featuring low-voltage technology
  - typical operating current of 1mA.
  - typical standby current of 1μA.
- Memory organization
  - SL24C02, 256 x 8 (2K bits)
  - SL24C04, 512 x 8 (4K bits)
  - SL24C08, 1024 x 8 (8K bits)
  - SL24C16, 2048 x 8 (16K bits)
  - SL24C32, 4096 x 8 (32K bits)
  - SL24C64, 8192 x 8 (64K bits)
- 2-wire serial interface, fully compatible with I²C bus
- I²C clock frequency: 1 MHz (at 5V), 400 kHz (at 1.8V, 2.5V, 2.7V)
- Schmitt trigger input noise suppression
- Hardware data write protection
- Internal write cycle (up to 5 ms)
- Byte write operation
- Page write: 8-byte page (SL24C02), 16-byte page (SL24C04/08/16), 32-byte page (SL24C32/64)
- Byte, random, and sequential read capabilities
- Automatic address increment
- ESD protection > 2.5 kV
- High reliability
  - erase/write cycles: 1 million times
  - data retention: 100 years
- 8-pin dip and 8-pin sop packages
- Lead-free process, RoHS compliant

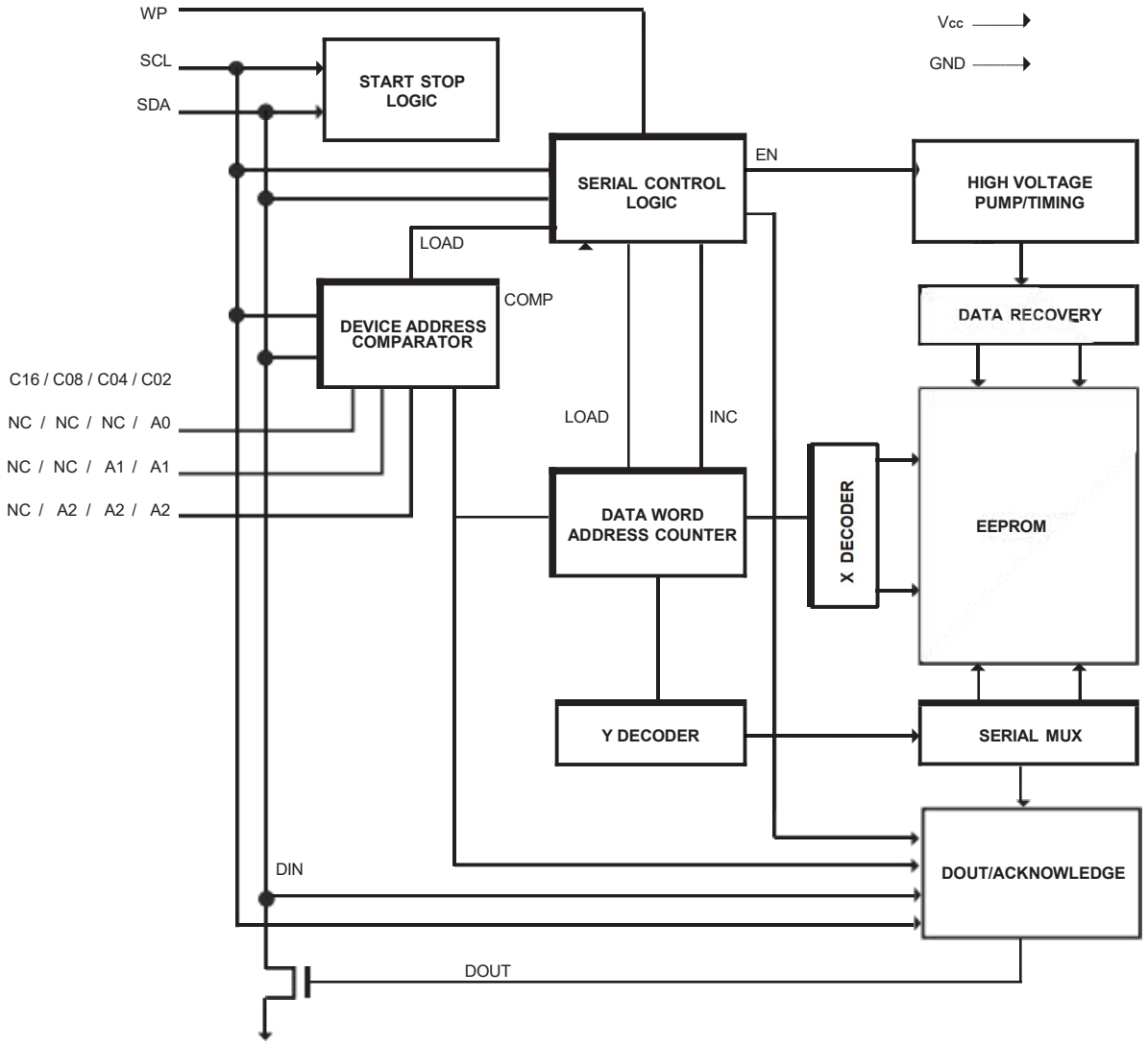
Application

- Smart instruments and meters
- Laptop computers
- Industrial control
- Automotive electronics
- Household appliances
- Communication equipment

Ordering information

Operating temperature range	Package		PN	Standard packaging quantity
-4 0 ℃~ + 8 5 ℃	S O P 8 L	lead-free	SL24C02D	4000 tape/reel
	D IP 8 L		SL24C02P	5 0tape/bulk
	S O P 8 L		SL24C04D	4000 tape/reel
	D IP 8 L		SL24C04P	5 0tape/bulk
	S O P 8 L		SL24C08D	4000 tape/reel
	D IP 8 L		SL24C08P	5 0tape/bulk
	S O P 8 L		SL24C16D	4000 tape/reel
	D IP 8 L		SL24C16P	5 0tape/bulk
	S O P 8 L		SL24C32D	4000 tape/reel
	D IP 8 L		SL24C32P	5 0tape/bulk
	S O P 8 L		SL24C64D	4000 tape/reel
	D IP 8 L		SL24C64P	5 0tape/bulk

Block diagram



Maximum ratings (exceeding maximum rated parameters may cause device damage)

Parameter	Symbol	Value	Unit
DC power supply voltage	V_{CC}	-0.3 ~ +6.5	V
input voltage	V_{IN}	-0.3 ~ V_{CC} +0.3	V
output voltage	V_{OUT}	-0.3 ~ VCC +0.3	V
stroage temperature	T_{STG}	-65 ~ +150	°C
ESD voltage(manikin)	V_{ESD}	2500	V
ESD voltage(machine model)		200	V

Operating conditions

Parameter	Symbol	Min	Max	Unit
DC power supply voltage	V_{CC}	1.8	5.5	V
operating temperature	T_A	-40	+85	°C

Pin capacitor (condition: T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V)

Parameter	Symbol	Text condition	Min	Max	Unit
input/output capacitance (SDA)	$C_{I/O}$	$V_{I/O}$ = 0V		8	pF
INPUT capacitance (A0, A1, A2, SCL)	C_{IN}	V_{IN} = 0V		6	pF

DC electrical characteristics

(condition: T_A = 0°C ~+70°C, V_{CC} = +1.8V ~+5.5V, unless otherwise specified)

Parameter	Symbol	Text condition		Min	Typ	Max	Unit
supply current	I_{CC}	V_{CC} =5V	100kHz read		0.4	1.0	mA
			100kHz write		2.0	3.0	mA
standby current	I_{SB}	V_{IN} = V_{CC} or GND				1.0	μA
input leakage current	I_{LI}	V_{IN} = V_{CC} or GND				3.0	μA
output leakage current	I_{LO}	V_{OUT} = V_{CC} or GND			0.05	3.0	μA
input low-level voltage	V_{IL}			-0.6		VCC ×0.3	V
input high-level voltage	V_{IH}			V_{cc}×0.7		VCC +0.5	V
output low-level voltage	$V_{OL}3$	V_{CC} =5.0V, I_{OL} = 3.0 mA				0.4	V
	$V_{OL}2$	V_{CC} =3.0V, I_{OL} = 2.1 mA				0.4	V
	$V_{OL}1$	V_{CC} =1.8V, I_{OL} = 0.15 mA				0.2	V

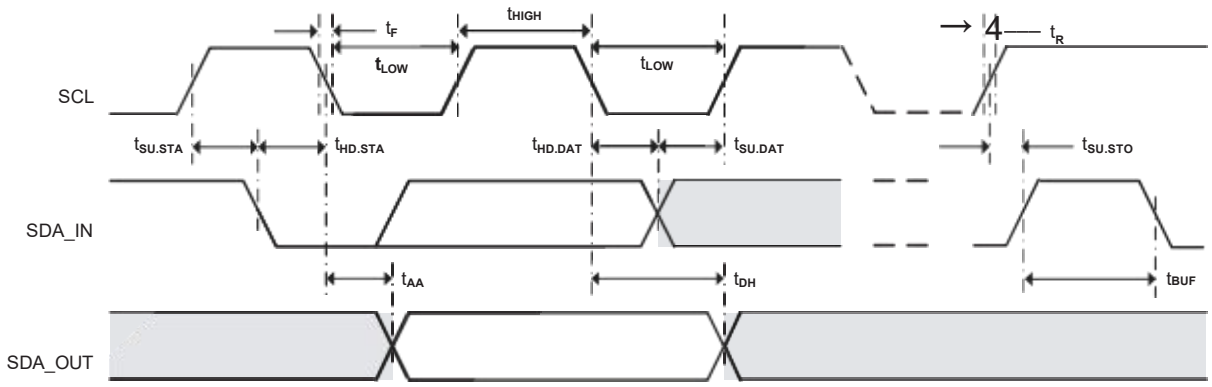
AC electrical characteristics

(condition: T_A = 0°C ~+70°C, V_{CC} = +1.8V ~+5.5V, C_L = 100 pF, unless otherwise specified)

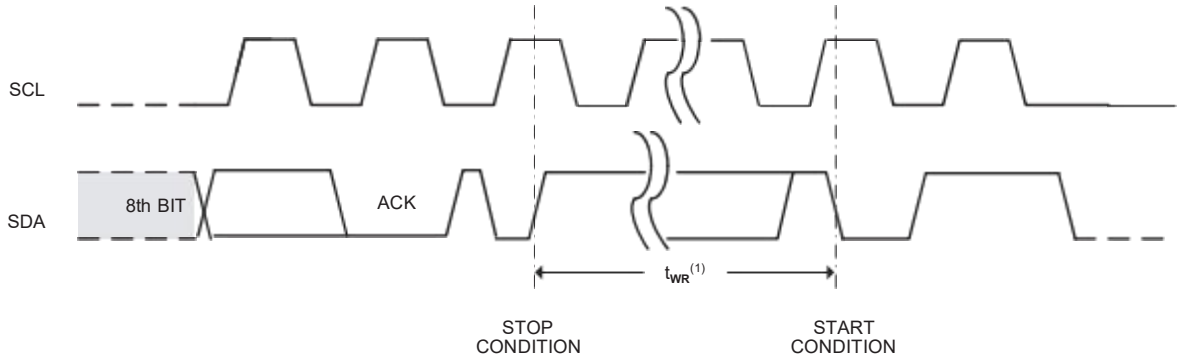
Parameter	Symbol	Text condition	Min	Typ	Max	Unit
clock frequency,SCL	f_{SCL}	V_{CC} =1.8V			400	kHz
		V_{CC} =5V			1000	
clock low pulse width	t_{LOW}	V_{CC} =1.8V	1.2			μs
		V_{CC} =5V	0.6			
clock high pulse width	t_{HIGH}	V_{CC} =1.8V	0.6			μs
		V_{CC} =5V	0.4			
noise suppression time	t_I	V_{CC} =1.8V			50	ns
		V_{CC} =5V			40	
clock falling edge to data valid output interval time	t_{AA}	V_{CC} =1.8V	0.05		0.9	μs
		V_{CC} =5V	0.05		0.55	
bus release time	t_{BUF}	V_{CC} =1.8V	1.2			μs
		V_{CC} =5V	0.5			

AC electrical characteristics

Parameter	Symbol	Text condition	Min	Typ	Max	Unit
setup time (for start conditions)	$t_{HD.STA}$	V_{CC} =1.8V	0.6			μs
		V_{CC} =5V	0.25			
hold time (for start conditions)	$t_{SU.STA}$	V_{CC} =1.8V	0.6			μs
		V_{CC} =5V	0.25			
data input hold time	$t_{HD.DAT}$		0			μs
data input setup time	$t_{SU.DAT}$		100			ns
input rise time	t_R				300	ns
input fall time	t_F	V_{CC} =1.8V			300	ns
		V_{CC} =5V			100	
setup time (for stop conditions)	$t_{SU.STO}$	V_{CC} =1.8V	0.6			μs
		V_{CC} =5V	0.25			
data output hold time	t_{DH}		50			ns
write cycle	t_{WR}				5	ms



Bus Timing



PS: The write cycle time twR is the time from the start of a valid stop condition for a write sequence to the end of the internal write cycle.

Write Cycle Timing

Pin Description

Pin NO.	Pin Name	Function
1	A0	address inputs. A2, A1, and A0 are device address input pins. the SL4C02/32/64 uses the A2, A1, and a input pins for the hardware address and can cascade up to 8 SL24C02/32/64 devices on the bus at the same time (see device addressing for details). SL24C04 uses a2 and A1 input pins for hardware address, four SL24C04 devices can be cascaded on the bus at the same time, A0 is a null pin and can be grounded. SL24C08 use A2 input pin as hardware address, two 24C08 devices can be cascaded on the bus at the same time, A0 and A1 are empty pins and can be grounded. SL24C16 no device address pin is used, up to one 16k device can be connected on the bus, A2, A1 and A0 are empty and can be grounded.
2	A1	
3	A2	
5	S_{DA}	serial address and data inputs/outputs S_{DA} is a bi-directional serial data transfer pin, open drain, requires external pull-up resistor to V_{cc} (10kΩ typical).
6	S_{CL}	serial clock input.SCL synchronous data transfer, rising edge data write, falling edge data read.
7	WP	write protect. the WP pin provides hardware data protection. when WP is grounded, normal data read/write operations are allowed; when WP is connected to V_{cc}, write protection is provided and the data is read only.
4	GND	ground
8	V_{CC}	positive power

Storage structure

Device Total Capacity (bits)	Total Capacity (bits)	Total Pages	Bytes/Page	Word Address Length
SL24C02	2K	32	8	8
SL24C04	4K	32	16	9
SL24C08	8K	64	16	10
SL24C16	16K	128	16	11
SL24C32	32K	128	32	12
SL24C64	64K	256	32	13

The SL24CXX supports the I2 C bus transfer protocol. I2 C is a bi-directional, two-wire serial communication interface, with a serial data line, SDA, and a serial clock line, SCL, both of which must be connected to the power supply through a pull-up resistor. A typical bus configuration is shown in Figure 4.

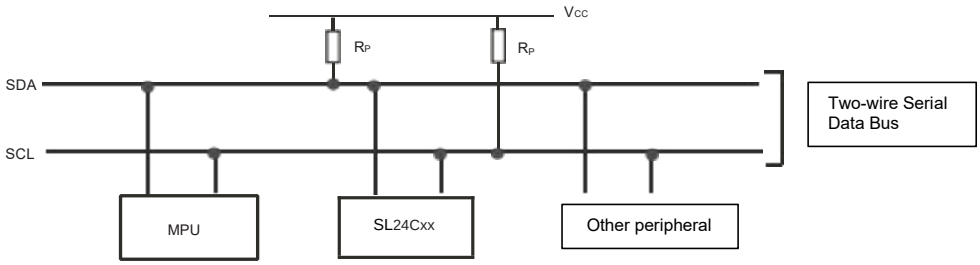


Figure 4. Typical 2-wire bus configuration

The device on the bus that sends data is called a transmitter, and the device that receives data is called a receiver. The device that controls the exchange of information is called the master, and the devices controlled by the master are called slaves. The master generates the serial clock SCL, controls the bus access state, and generates the START and STOP conditions. The SL24CXX operates as a slave device on the I2C bus.

Data transfers can only be initiated when the bus is idle. Each data transfer starts with a START condition and ends with a STOP condition.

Each data transfer starts with the START condition and ends with the STOP condition. There is no limit to the number of bytes of data between the two, which is determined by the master device on the bus. The information is transmitted in bytes (8 bits) and the receiver generates an answer at bit 9.

Start and stop conditions

When both the data and clock lines are high, the bus is said to be in an idle state. When SCL is high, the falling edge of SDA (high to low) is called the start condition (START, abbreviated as S), and the rising edge of SDA (low to high) is called the stop condition (STOP, abbreviated as P). See Figure 5.

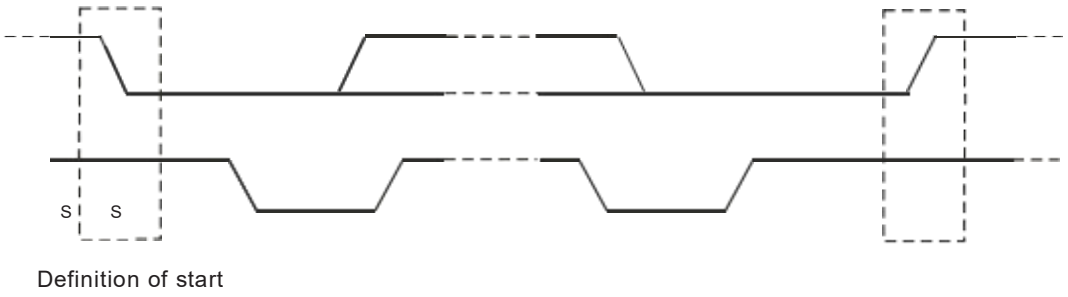
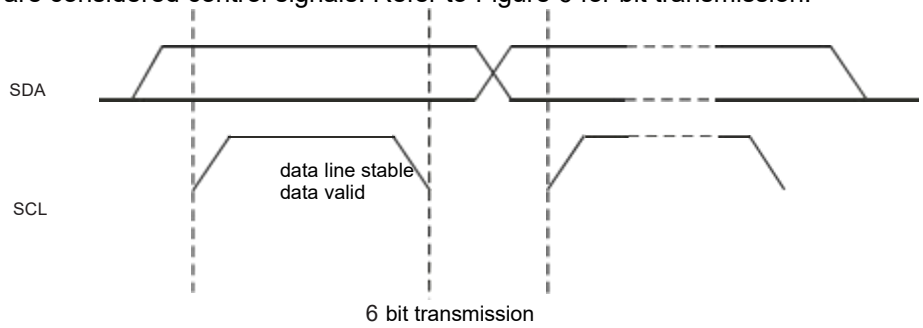


Figure 5. Definition of start and stop conditions

Detailed operating instructions

Bit transmission

Each clock pulse transmits one bit of data. When SCL is high, SDA must remain stable, as changes in SDA at this time are considered control signals. Refer to Figure 6 for bit transmission.



Response

The receiver on the bus generates an acknowledgment for each received byte, and the master device must generate an additional clock pulse accordingly. See Figure 7.

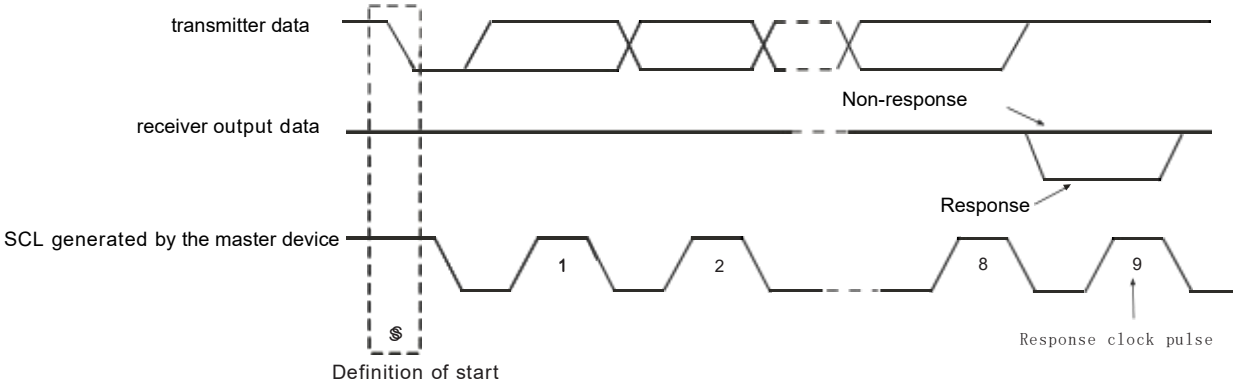


Figure7. I^2C bus response

The receiver pulls the SDA line low to indicate acknowledgment and maintains a stable low level during the acknowledgment pulse period. When the master device acts as a receiver, it must send a signal to the transmitter indicating the end of data transfer. Therefore, during the acknowledgment pulse period following the last byte, it does not generate an acknowledgment signal (does not pull SDA low). In this case, the transmitter must release the SDA line to high so that the master device can generate a stop condition.

Device addressing

- After enabling the start condition for chip read/write operations, EEPROM requires an 8-bit device address information (see Figure 8).
- The device address information consists of a sequence of '1' and '0', where the first 4 bits are as shown in the figure, and are identical for all serial EEPROM.
- For SL 24C02/32/64, the subsequent 3 bits A2, A1, and A0 are device address bits that must match the hardware input pins.
- For SL 24C04, the subsequent 2 bits A2 and A1 are device address bits, and the remaining bit is the page address bit. A2 and A1 must match the hardware input pins, while A0 is a no-connect pin.
- For SL 24C08, the subsequent 1 bit A2 is a device address bit, and the remaining 2 bits are page address bits. A2 must match the hardware input pin, while A1 and A0 are no-connect pins.
- For SL 24C16, there are no device address bits; all 3 bits are page address bits, and A2, A1, and A0 are no-connect pins.
- The LSB of the device address information determines the read/write operation: high for read operation and low for write operation.
- If the device addresses match, the EEPROM will output an acknowledge '0'. If they do not match, it returns to standby mode.

SL 24C02/32/64	1	0	1	0	A2	A1	A0	R/W
	MSB							LSB
SL 24C04	1	0	1	0	A2	A1	P0	R/W
SL 24C08	1	0	1	0	A2	P1	P0	R/W
SL 24C16	1	0	1	0	P2	P1	P0	R/W

8 device address

Device operation

Standby mode

EEPROM features low-power standby mode under the following conditions:
(1)Power supply turn-on;
(2) Reception of a stop condition and completion of any internal operations.

Storage reset

After interruptions, power loss, or system reset in the protocol, the I2C bus can be reset using the following steps:

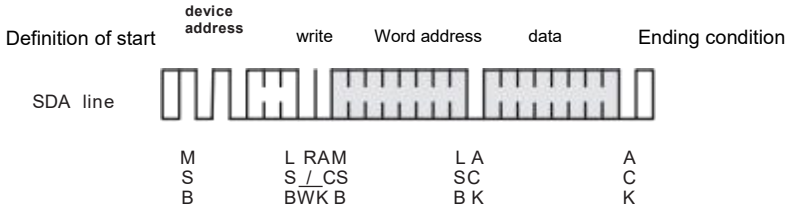
(1) Generate 9 clock cycles.
(2) Keep SDA high while SCL is high.
(3) Generate a start condition.

rite operation

Byte Write

A write operation requires sending the device address and receiving an ACK (acknowledgement) response. Following this, an 8-bit word address is transmitted. Upon receiving this address, the EEPROM responds with '0'. Subsequently, an 8-bit data byte is sent. After receiving the data byte, the EEPROM responds with '0'. The master device must then send a stop condition to terminate the write sequence.

At this point, the EEPROM enters the internal write cycle t_{WR}, during which all inputs are invalid as the data is written into non-volatile memory. The EEPROM will acknowledge completion only after the write cycle is finished (see Figure 9).



9 Byte Write

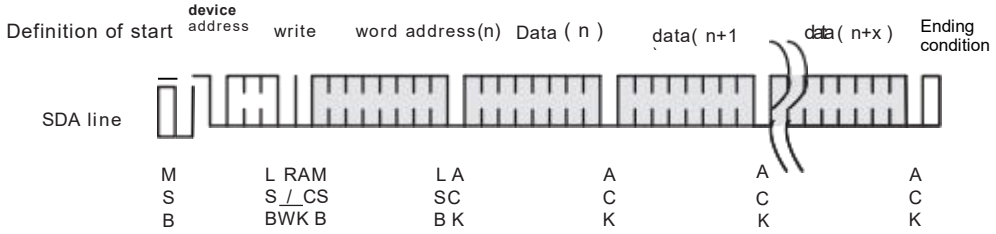
Detailed operating instructions

Page write

SL24C02 devices perform page writes in 8-byte pages, SL24C04/08/16 devices perform page writes in 16-byte pages, and SL24C32/64 devices perform page writes in 32-byte pages.

Page write initialization is similar to byte write, except the master device does not send a stop condition after the first data byte. Instead, the EEPROM acknowledges each data byte with a "0". Finally, the master device sends a stop condition to terminate the write sequence (refer to Figure 10).

Upon receiving each data byte, the low 3 bits (SL24C02), 4 bits (SL24C04/08/16), or 5 bits (SL24C32/64) of the word address automatically increment, while the high address bits remain unchanged within the current page. When the internally generated word address reaches the boundary address of the page, subsequent data bytes will be written starting from the beginning of that page. If more than 8 (SL24C02), 16 (SL24C04/08/16), or 32 (SL24C32/64) data bytes are transferred to the EEPROM, the word address will wrap around to the first byte of that page, overwriting previous bytes.

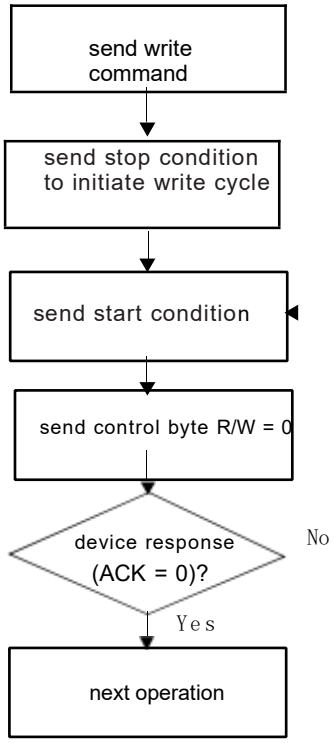


10 page write

Acknowledge query

Once the internal write cycle is initiated, EEPROM inputs are invalid. At this point, an acknowledge query can be initiated: send a start condition and device address (with the read/write bit indicating the desired operation). The EEPROM will only acknowledge with "0" after the internal write cycle is completed. After this, read/write operations can proceed.

Refer to Figure 11 for the acknowledge query process.



11 acknowledge query process

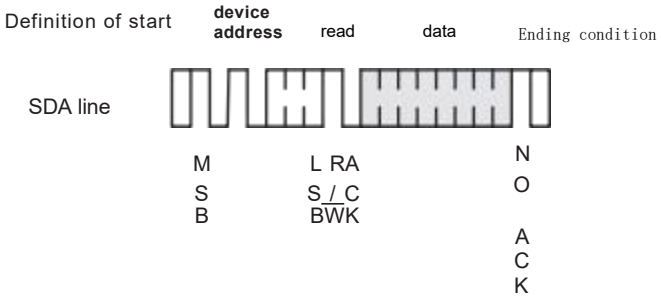
Read operation

Read operations initialize similarly to write operations, except the read/write bit in the device address should be set to '1'. There are three different read operation modes: current address read, random read, and sequential read.

Current address read

The internal address counter retains the value of the last accessed address plus one from the previous access. This address is retained as long as the chip has power. When reading reaches the last byte of the last page, the address wraps around to 0; when writing to the last byte of a page, the address wraps around to the first byte of that page.

After transmitting the device address (with the read/write bit set to '1') and receiving an ACK from the EEPROM, the data from the current address is sent out synchronized with the clock. The master device does not need to acknowledge with '0', but it must send a stop condition (see Figure 12).

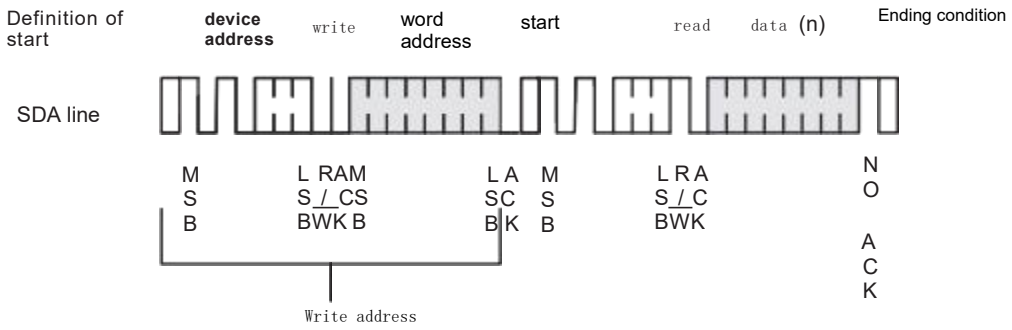


12 current address read

Random read

For random read, the master device first writes a target word address. Once the EEPROM receives the device address and word address and acknowledges with ACK, the master device generates a repeated start condition.

Next, the master device sends the device address (with the read/write bit set to '1'). The EEPROM acknowledges with ACK and sends out data synchronized with the clock. The master device does not need to acknowledge with '0', but it must send a stop condition (see Figure 13).

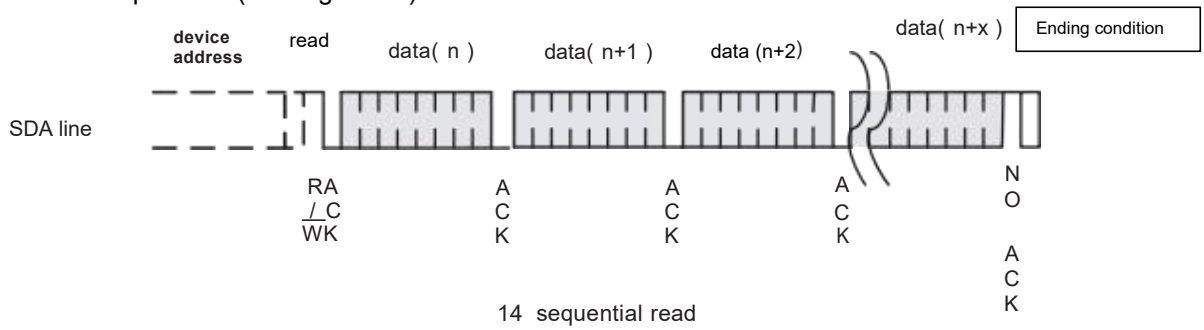


13 random read

Sequential read

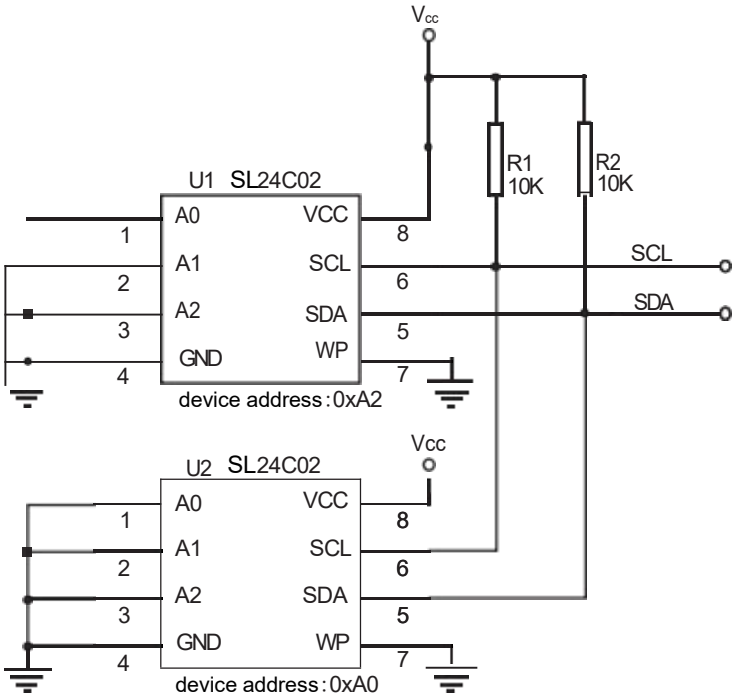
Sequential read can be initiated using either 'current address read' or 'random read'. Upon receiving each data byte, the master device acknowledges with ACK. As long as the EEPROM receives ACK, it automatically increments the word address and continues to transmit subsequent data synchronized with the clock. If the end of the memory address is reached, the address automatically wraps around to 0, allowing sequential data reading to continue.

The master device does not acknowledge with '0'; instead, it sends a stop condition to terminate the sequential read operation (see Figure 14).



14 sequential read

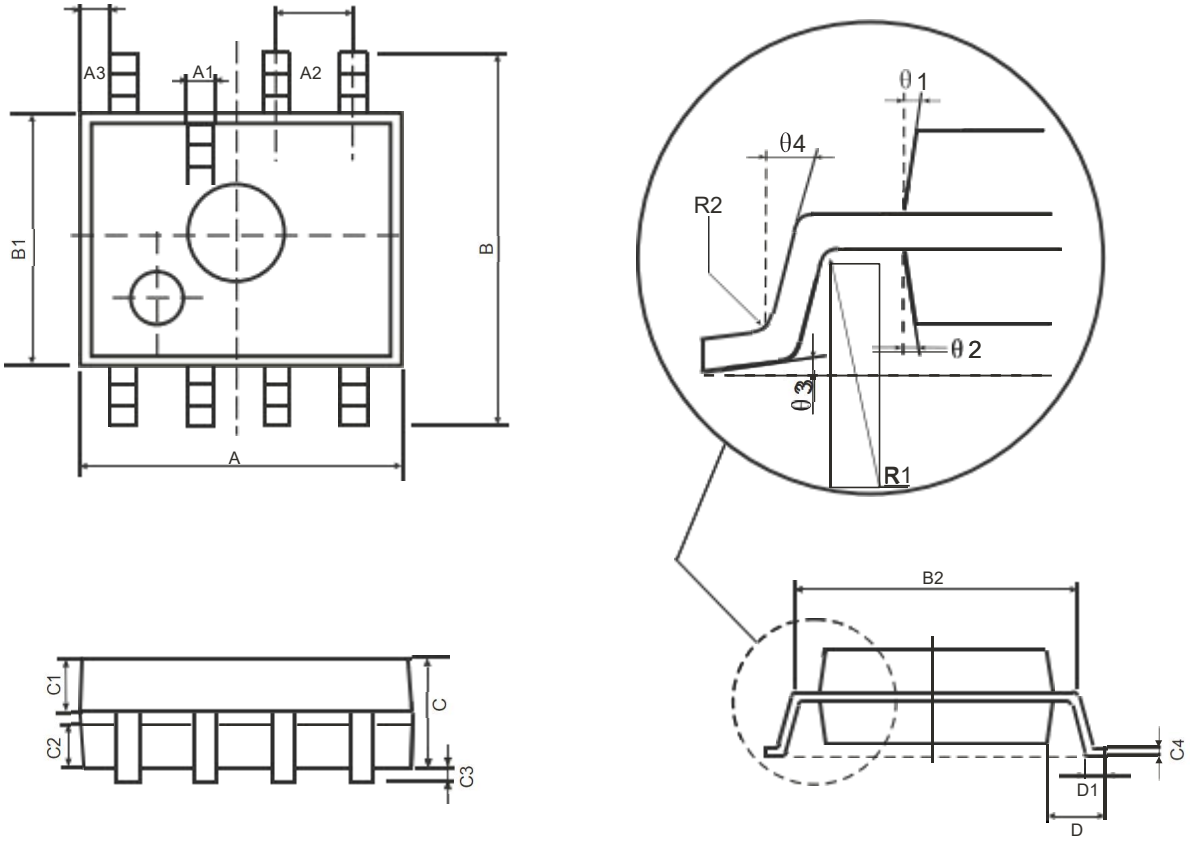
Typical Application



15 Cascade of EEPROM

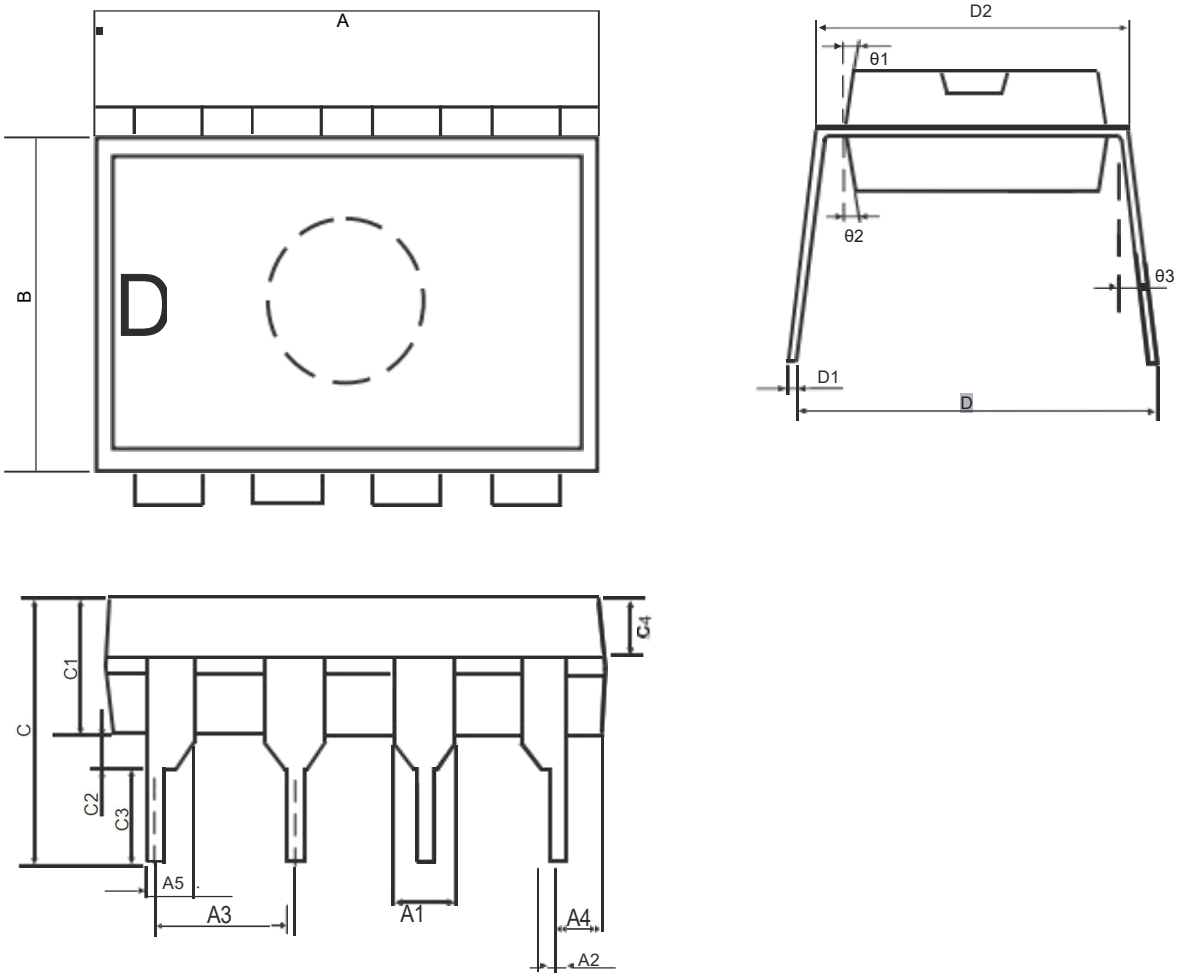
Package dimension

SOP8L



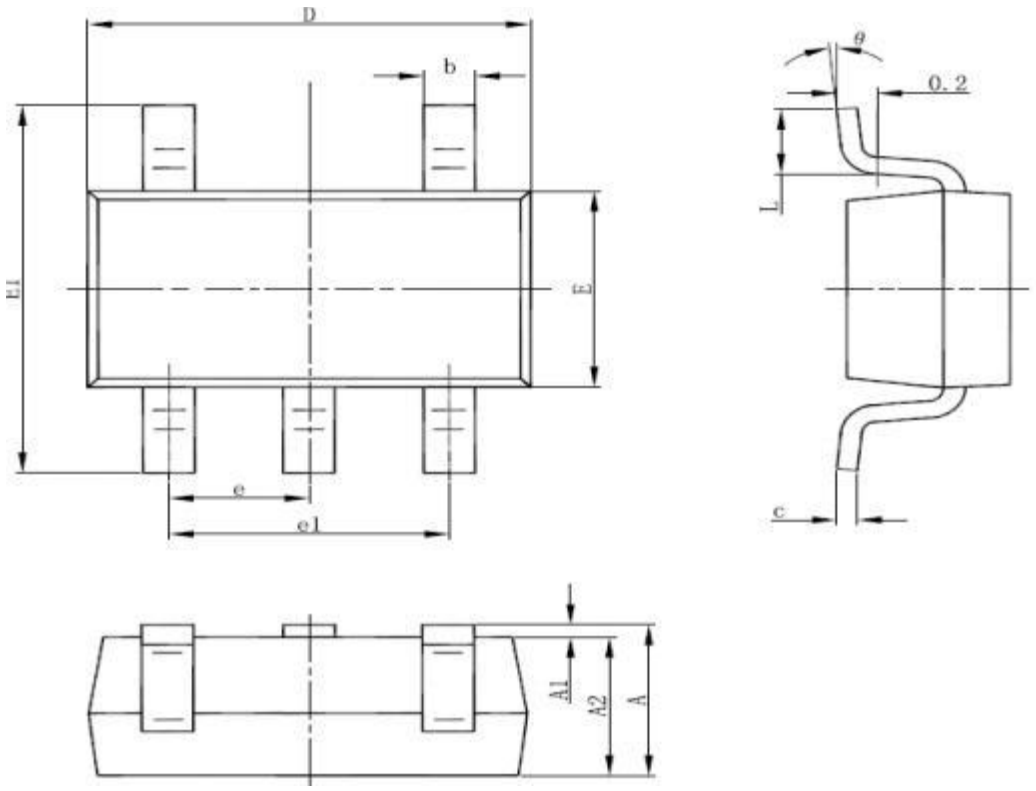
Symbol	Size(mm)		Symbol	Size(mm)	
	Min	Max		Min	Max
A	4.95	5.15	C3	0.05	0.20
A1	0.37	0.47	C4	0.20(Typ)	
A2	1.27(Typ)		D	1.05(Typ)	
A3	0.41(Typ)		D1	0.40	0.60
B	5.80	6.20	R1	0.07(Typ)	
B1	3.80	4.00	R2	0.07(Typ)	
B2	5.0(Typ)		θ1	17°	
C	1.30	1.50	θ2	13°	
C1	0.55	0.65	θ3	4°	
C2	0.55	0.65	θ4	12°	

DIP8L



Symbol	Size(mm)		Symbol	Size(mm)	
	Min	Max		Min	Max
A	9.30	9.50	C2	0.5	
A1	1.524		C3	3.3	
A2	0.39	0.53	C4	1.57	
A3	2.54		D	8.20	8.80
B	0.66		D1	0.20	0.35
B1	0.99		D2	7.62	7.87
B2	6.3	6.5	θ1	8	
C	7.2		θ2	8	
C1	3.30	3.50	θ3	5	

SOT-23-5 package outline dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.900	0.028	0.035
A1	0.000	0.100	0.000	0.004
A2	0.700	0.800	0.028	0.031
b	0.350	0.500	0.014	0.020
c	0.080	0.200	0.003	0.008
D	2.820	3.020	0.111	0.119
E	1.600	1.700	0.063	0.067
E1	2.650	2.950	0.104	0.116
e	0.95 (BSC)		0.037 (BSC)	
e1	1.90 (BSC)		0.075 (BSC)	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°