Description

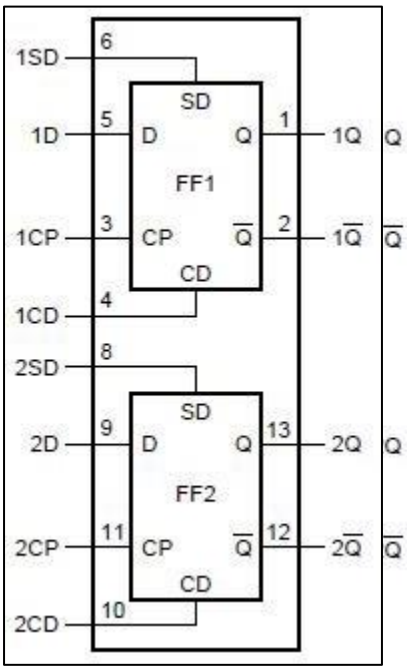
CD4013 is a dual D-type flip-flop, consisting of two identical, independent data-triggered flip-flops. Each flip-flop has independent data (D), set (SD), reset (CD), clock input (CP), and Q and Q' complementary outputs.

This device can function as a shift register and, by connecting the Q output to the data input, can be used in counters and triggers. When triggered on the rising edge of the clock, the logic level applied to the D input is transferred to the Q output. Set and reset operations are asynchronous with respect to the clock and are activated by a high level on the set or reset line, respectively.

The recommended operating voltage (V_{DD}) for CD4013 is between 3V and 15V. Input ports must be connected to V_{DD}, V_{SS}, or other input pins. Its main characteristics include:

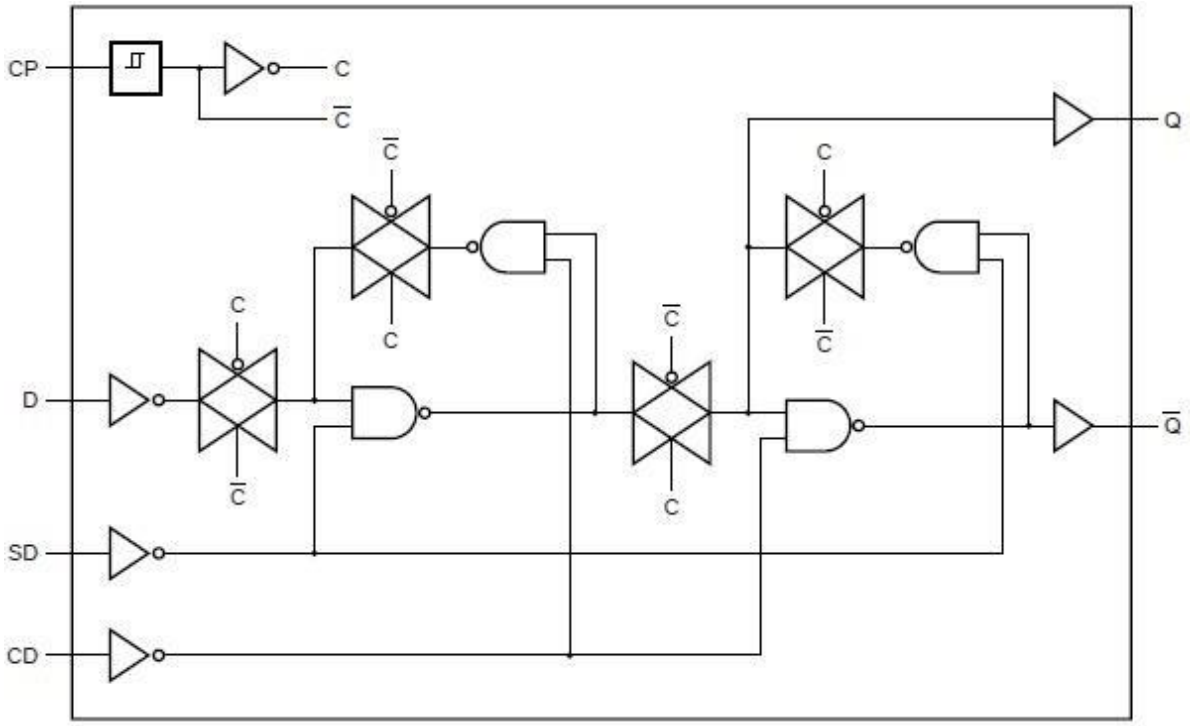
- Wide clock rising and falling edges
- Fully static operation
- Operates under three reference voltages: 5v, 10v, and 15v
- Standard symmetric output characteristics
- Provides a wide temperature range: -40°c to +85°c
- Complies with jedec standard jesd13-b
- Applications include automation and industrial fields
- Ring counters
- Registers
- Fixed triggers
- Package type: Sop-14

Functional Block Diagram and Pin Description

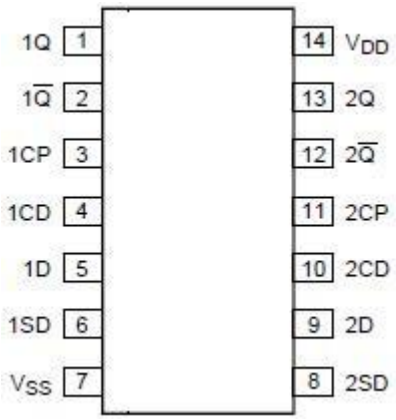


Functional Block Diagram

Logic diagram (single trigger)



Pinout diagram



Pin description and structural schematic

Pin Number	Pin Name	Function
1	1Q	logic positive input
2	1 $\overline{Q}$	logic negative input
3	1CP	clock input (low-to-high clock triggering edge active)
4	1CD	asynchronous reset input (active high)
5	1D	data input
6	1SD	asynchronous set input (active high)
7	VSS	system ground (0V)
8	2SD	asynchronous set input (active high)
9	2D	data input
10	2CD	asynchronous reset input (active high)
11	2CP	clock input (low-to-high clock edge triggered)
12	2 $\overline{Q}$	logic negative input
13	2Q	logic positive input
14	VDD	system power

Truth table and Logical relationships

Control port			Input	output	
n_{SD}	n_{CD}	n_{CP}	n_D	n_Q	$n_{\overline{Q}}$
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H
L	L	↑	L	L	H
L	L	↑	H	H	L

ps：H = active high; L = active low; X = non-consider ; ↑= clock rise

Electrical Characteristics

Maximum ratings (Unless otherwise specified, T_{amb}=25℃,V_{ss} = 0V)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
power supply voltage	V_{DD}			-0.5	-	+15	V
input clamping current	I_{IK}	V_I < -0.5 V or V_I > V_{DD} + 0.5 V		-	-	±10	mA
input voltage	V_I			-0.5	-	V_{DD}+0.5	V
output clamping current	I_{ok}	V_O < -0.5 V or V_O > V_{DD} + 0.5 V		-	-	±10	mA
input/output current	$I_{I/O}$			-	-	±10	mA
power supply current	I_{DD}			-	-	50	mA
operating environment temperature	T_{amb}			-40	-	+85	℃
storage temperature	T_{stg}			-65	-	+150	℃
soldering temperature	T_L	10 second	DIP		245		℃
			SOP		250		

Recommended operating conditions

Parameter	Symbol	Condition	Min	Max	Uint
power supply voltage	V_{DD}		3	15	V
input voltage	V_i		0	V_{DD}	V
operating environment temperature	T_{amb}		-40	+85	℃
input rise/fall rate	$\Delta t/\Delta V$	V_{DD} = 5V	-	3.75	ns/V
		V_{DD} = 10V	-	0.5	ns/V
		V_{DD} = 15V	-	0.08	ns/V

Electrical characteristics

DC parameters 1（Unless otherwise specified, T_{amb}=25℃, V_{SS}=0V, V_I = V_{SS} or V_{DD} ）

Parameter	Symbol	Text condition			Min	Typ	Max	Uint
		V_O(V)	V_{in}(V)	V_{DD}(V)				
static current	I_{DD} max	-	0.5	5	-	0.02	1	uA
		-	1	10	-	0.02	2	
		-	1.5	15	-	0.02	4	
		-	-	-	-	-	-	
low-level output current	I_{OL} min	0.4	0.5	5	0.51	1	-	mA
		0.5	1	10	1.3	2.6	-	
		1.5	1.5	15	3.4	6.8	-	
high-level output current	I_{OH} min	4.6	0.5	5	-0.51	-1	-	
		2.5	0.5	5	-1.6	-3.2	-	
		9.5	1	10	-1.3	-2.6	-	
		13.5	1.5	15	-3.4	-6.8	-	
low-level output voltage	V_{OL} max	-	0.5	5	-	0	0.05	V
		-	1	10	-	0	0.05	
		-	1.5	15	-	0	0.05	
high-level output voltage	V_{OH} min	-	0.5	5	4.95	5	-	
		-	1	10	9.95	10	-	
		-	1.5	15	14.95	15	-	
low-level input voltage	V_{IL} max	0.5, 4.5	-	5	-	-	1.5	
		1, 9	-	10	-	-	3	
		1.5, 13.5	-	15	-	-	4	
high-level input voltage	V_{IH} min	0.5, 4.5	-	5	3.5	-	-	
		1, 9	-	10	7	-	-	
		1.5, 13.5	-	15	11	-	-	
input current	I_{IN} max	-	0.18	18	±10-5	±1		uA

DC parameters（Unless otherwise specified，V_{SS}=0V，V_I=V_{SS} or V_{DD}）

Parameter	Symbol	Text condition			Temperature		Unit
		V_O(V)	V_{in}(V)	V_{DD}(V)	-40	+85	
Static current	I_{DD} max	-	0.5	5	1	30	uA
		-	1	10	2	60	
		-	1.5	15	4	120	
		-	-	-	-	-	
Low-level output current	I_{OL} min	0.4	0.5	5	0.61	0.42	mA
		0.5	1	10	1.5	1.1	
		1.5	1.5	15	4	2.8	
High-level output current	I_{OH} min	4.6	0.5	5	-0.61	-0.42	
		2.5	0.5	5	-1.8	-1.3	
		9.5	1	10	-1.5	-1.1	
		13.5	1.5	15	-4	-2.8	
Low-level output voltage	V_{OL} max	-	0.5	5	0.05		V
		-	1	10	0.05		
		-	1.5	15	0.05		
High-level output voltage	V_{OH} min	-	0.5	5	4.95		
		-	1	10	9.95		
		-	1.5	15	14.95		
Low-level input voltage	V_{IL} max	0.5, 4.5	-	5	1.5		
		1, 9	-	10	3		
		1.5, 13.5	-	15	4		
High-level input voltage	V_{IH} min	0.5, 4.5	-	5	3.5		
		1, 9	-	10	7		
		1.5, 13.5	-	15	11		
Input current	I_{IN} max	-	0.18	08	±0.1	±1	uA

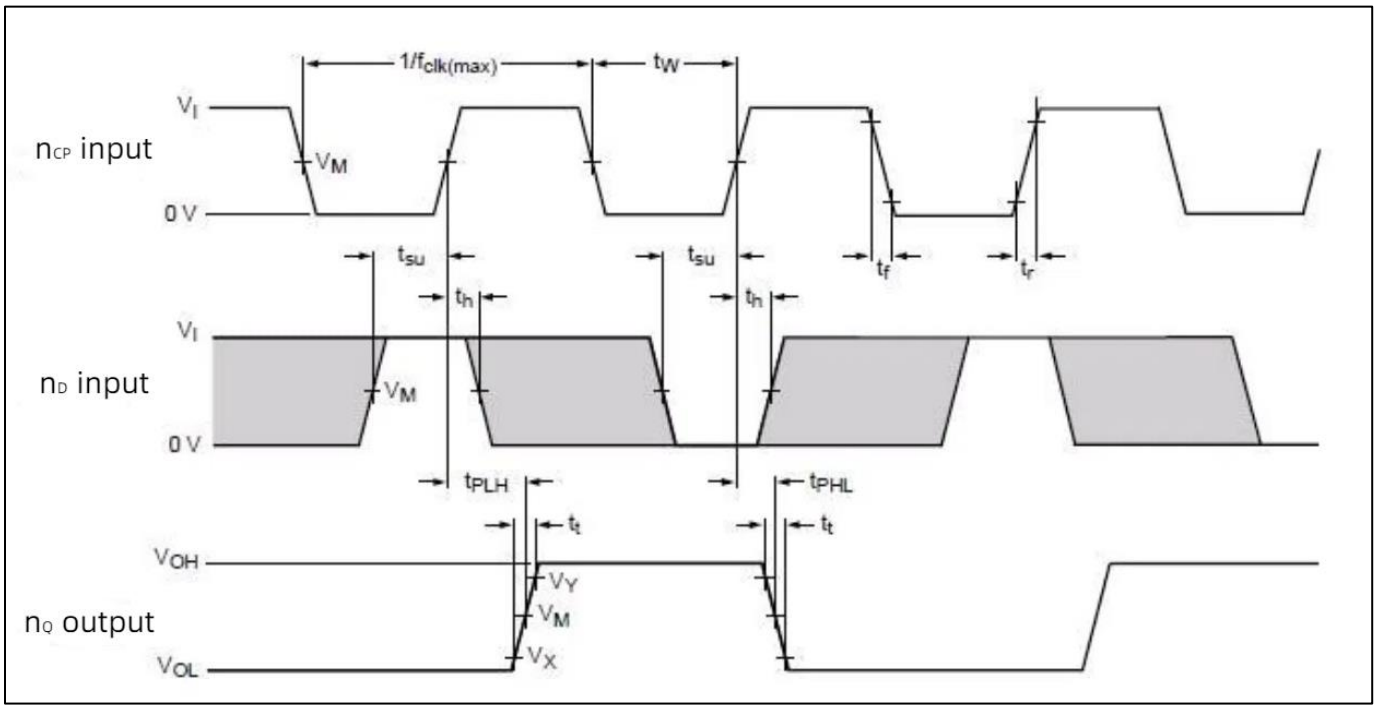
AC parameters（Unless otherwise specified, T_{amb}=25℃, input t_r,t_f = 20ns,C_L = 50pF,R_L = 20KΩ）

Parameter	Symbol	Text condition V_{DD}(V)	Min	Typ	Max	Uint
clock to Q, ¯Q output propagation delay	t_{PHL}, t_{PLH}	5	--	150	300	ns
		10	--	65	130	
		15	--	45	90	
set to Q or reset to ¯Q rising delay	t_{PLH}	5	--	150	300	ns
		10	--	65	130	
		15	--	45	90	
set to ¯Q or reset to Q falling delay	t_{PHL}	5	--	200	400	ns
		10	--	85	170	
		15	--	60	120	
transition time	t_{THL}, t_{TLH}	5	--	100	200	ns
		10	--	50	100	
		15	--	40	80	
maximum clock input frequency	f_{CL}	5	3.5	7	--	MHZ
		10	8	16	--	
		15	12	24	--	
minimum clock pulse width	t_W	5	--	70	140	ns
		10	--	30	60	
		15	--	20	40	
minimum set or reset pulse width	t_W	5	--	90	180	ns
		10	--	40	80	
		15	--	25	50	
minimum data setup time	t_s	5	--	20	40	ns
		10	--	10	20	
		15	--	7	150	
minimum data hold time	t_H	5	--	2	5	ns
		10	--	2	5	
		15	--	2	5	
clock input rise/fall time	tr_{CL}, tf_{CL}	5	--	--	15	ns
		10	--	--	10	
		15	--	--	5	
input capacitance	C_{in}	--	--	5	7.5	pF

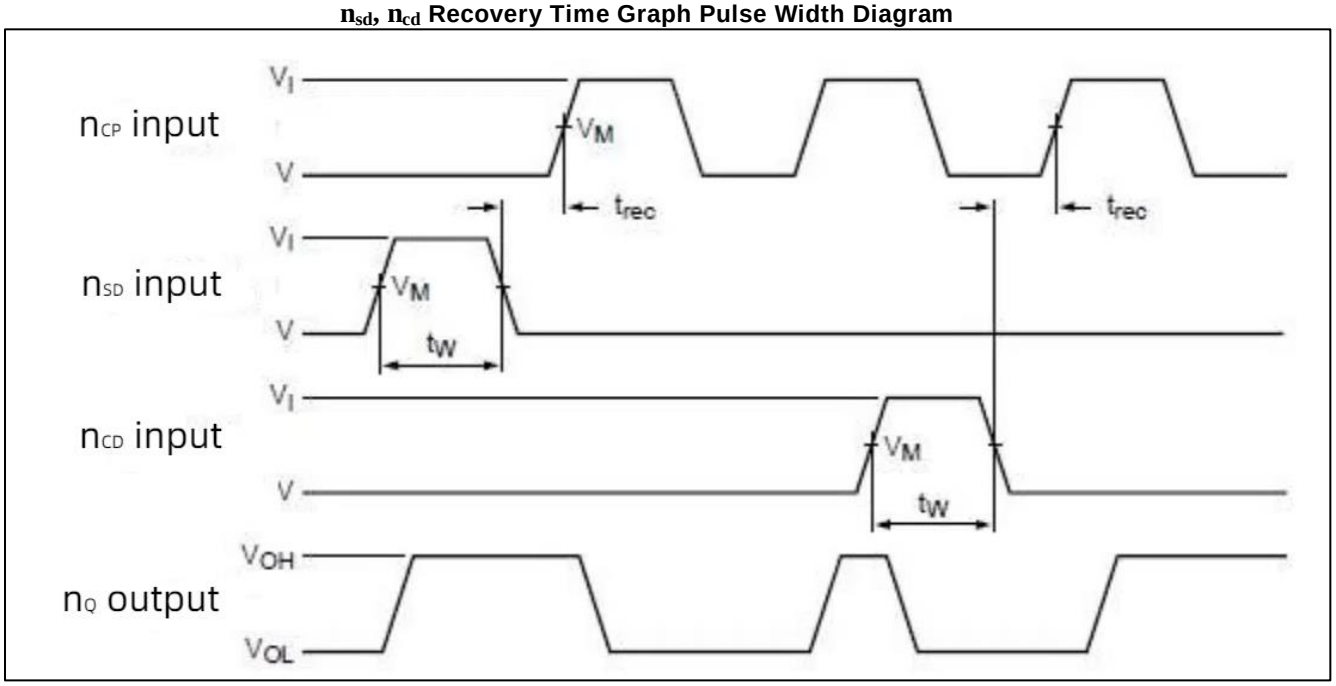
Test circuit

Ac test circuit

Data setup time data hold time minimum clock pulse width propagation delay and transition time



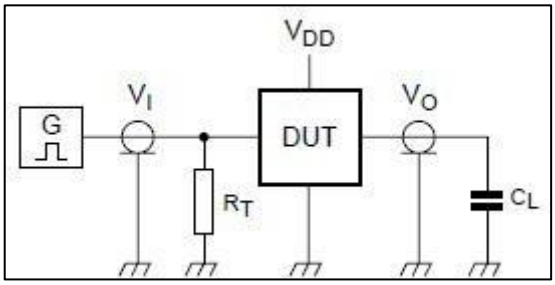
n_{sd}, n_{cd} Recovery Time Graph Pulse Width Diagram



Ps：texting point

Power Supply Voltage	Input	Output		
V_{DD}	V_M	V_M	V_X	V_Y
5 V to 15V	$0.5V_{DD}$	$0.5V_{DD}$	$0.1V_{DD}$	$0.9V_{DD}$

Switching Characteristics Test Circuit Diagram



PS:

CL：Load capacitance includes fixture and probe capacitance

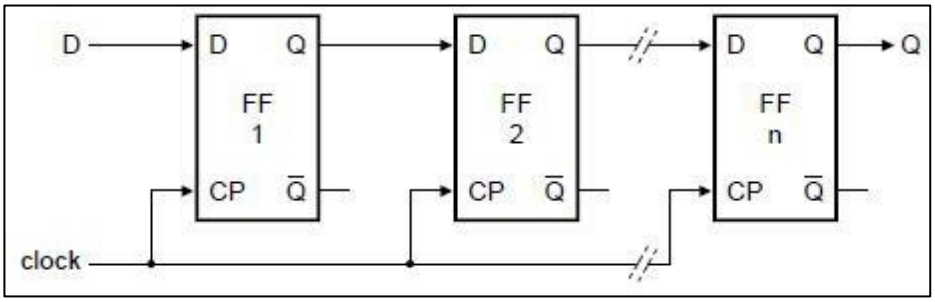
RT：Terminal resistor must match the output impedance of the signal source

Texting point

Power Supply Voltage	Input		Output
V_{DD}	V_I	tr,tf	C_L
5V to 15V	V_{ss} or V_{DD}	≤20 ns	50pF

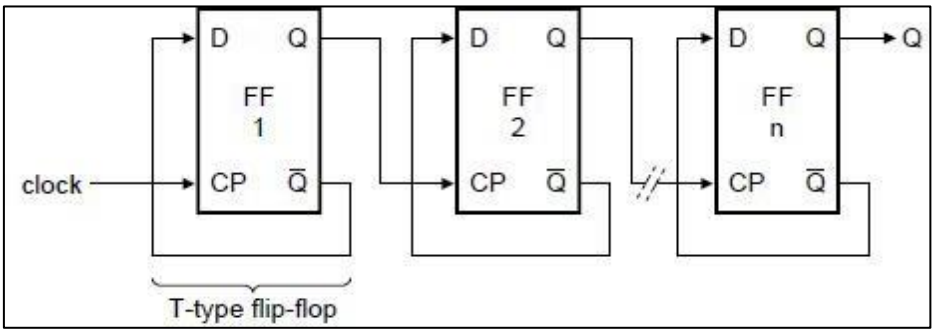
Typical Application Circuit And Description

Application Circuit 1



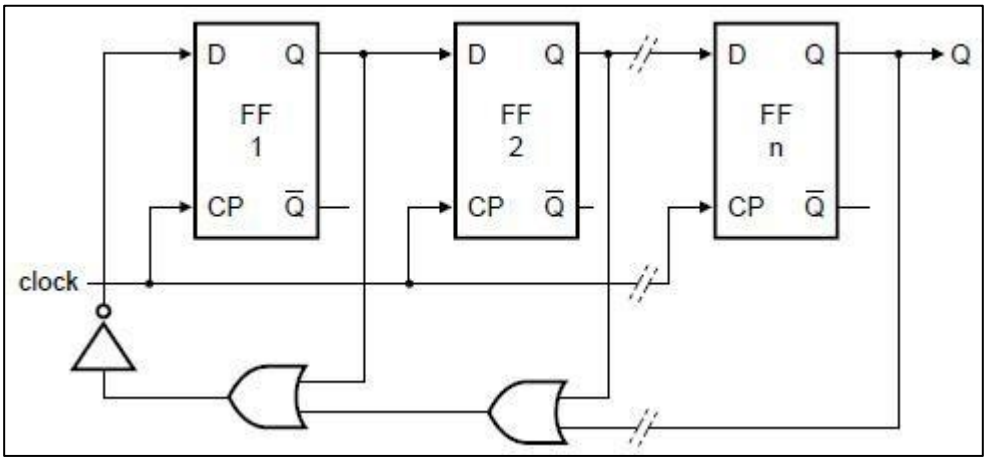
n-stage shift register

Application circuit 2



binary ring adder

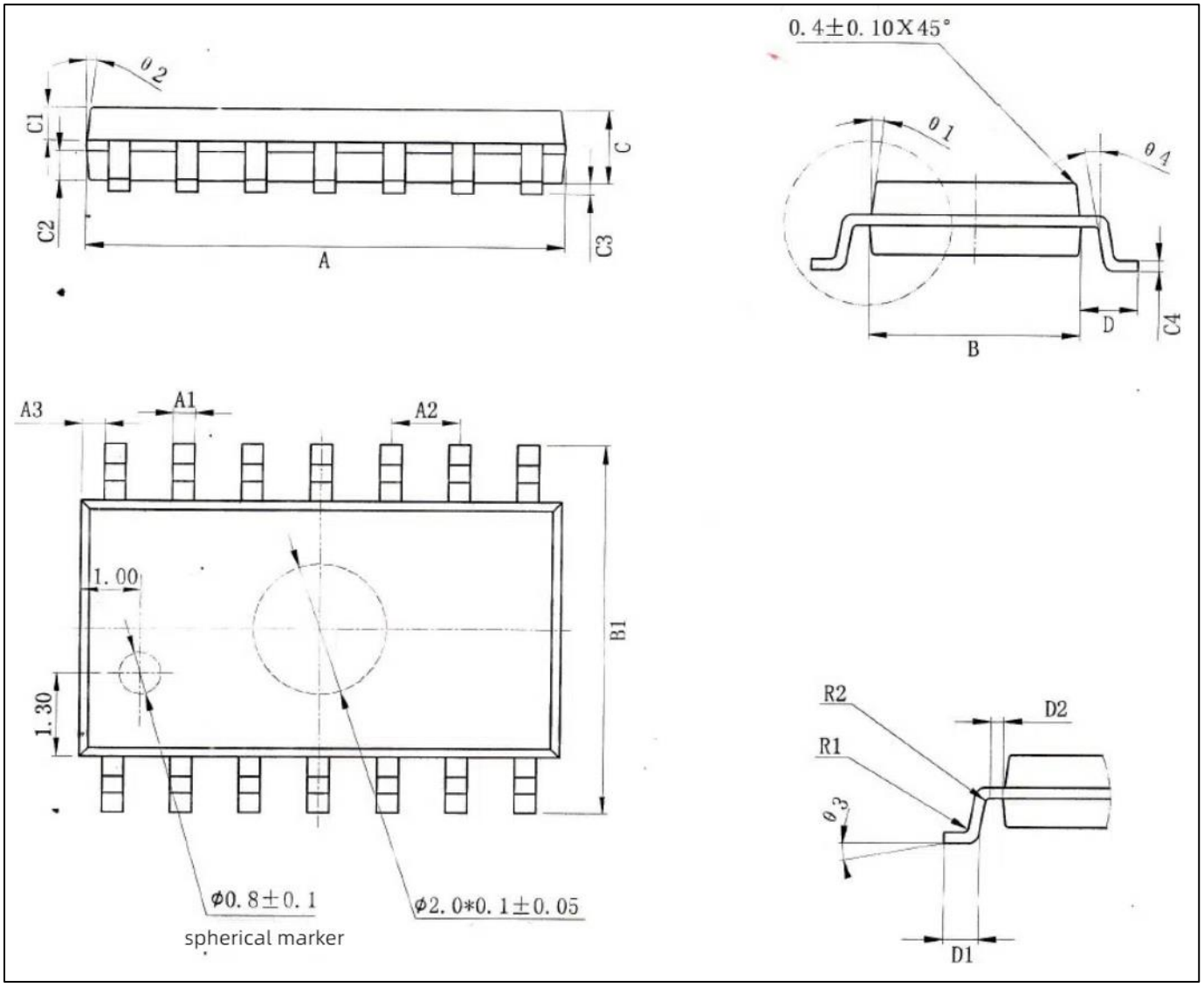
Application circuit 3



improved ring counter

Outline package diagram

SOP14



Symbol	Size（mm）		Symbol	Size（mm）	
	Min	Max		Min	Max
A	8.55	8.75	C4	0.203	0.233
A1	0.356	0.456	D	0.95	1.15
A2	1.27TYP		D1	0.40	0.70
A3	0.302TYP		D2	0.20TYP	
B	3.80	4.00	R1	0.20TYP	
B1	5.80	6.20	R2	0.20TYP	
C	1.40	1.60	Θ1	8°~12°TYP	
C1	0.60	0.70	Θ2	8°~12°TYP	
C2	0.52	0.62	Θ3	0°~8°	
C3	0.05	0.25	Θ4	4°~12°	