

600V High and Low Side Driver

PRODUCT SUMMARY

- V_{OFFSET} 600 V max.
- $I_{\text{O+/-}}$ 1 A / 1.6 A
- V_{OUT} 10 V - 20 V
- $t_{\text{on/off}}$ (typ.) 140 ns/140 ns
- **Delay Matching (typ.)** 10 ns

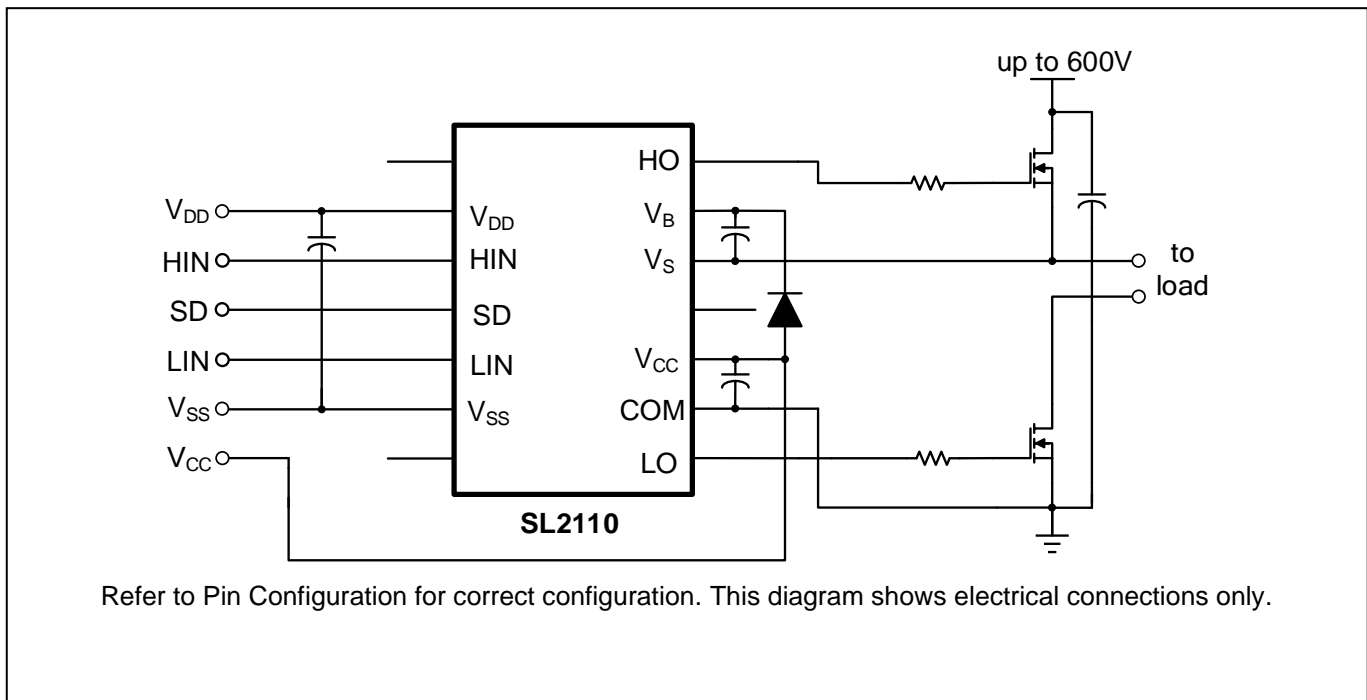
GENERAL DESCRIPTION

The SL2110 is a high voltage, high speed power MOSFET and IGBT drivers with independent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

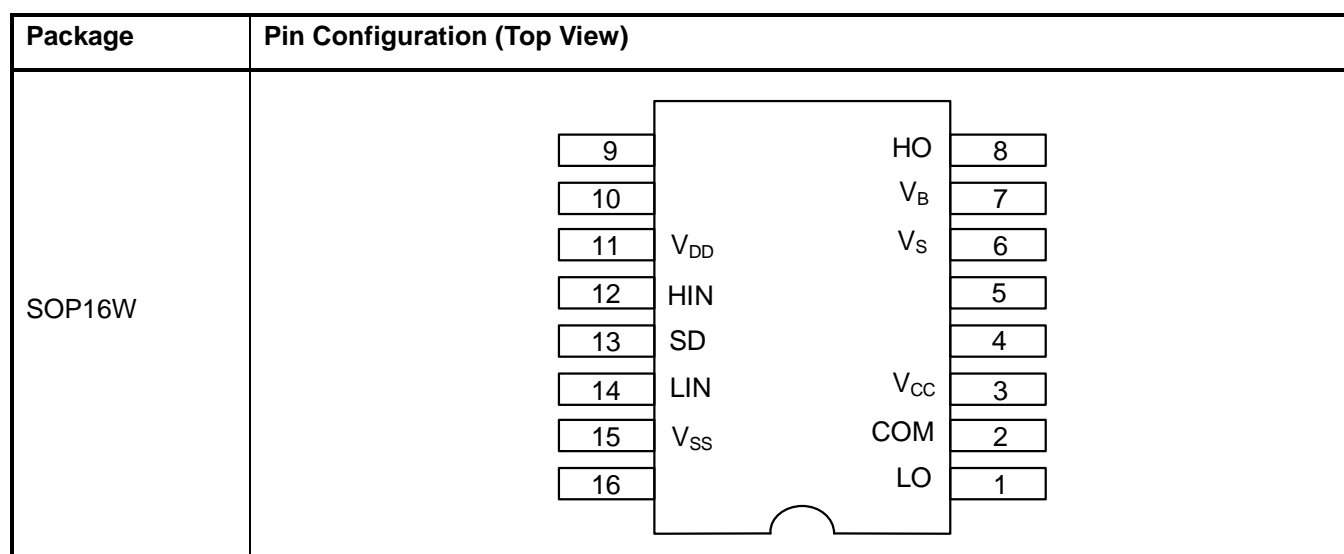
FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- Logic and power ground +/- 5V offset
- Cross-conduction prevention logic
- Schmitt-triggered inputs with pull-down
- Cycle-by-cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- RoHS compliant
- SOP16W package

TYPICAL APPLICATION CIRCUIT



PIN CONFIGURATION



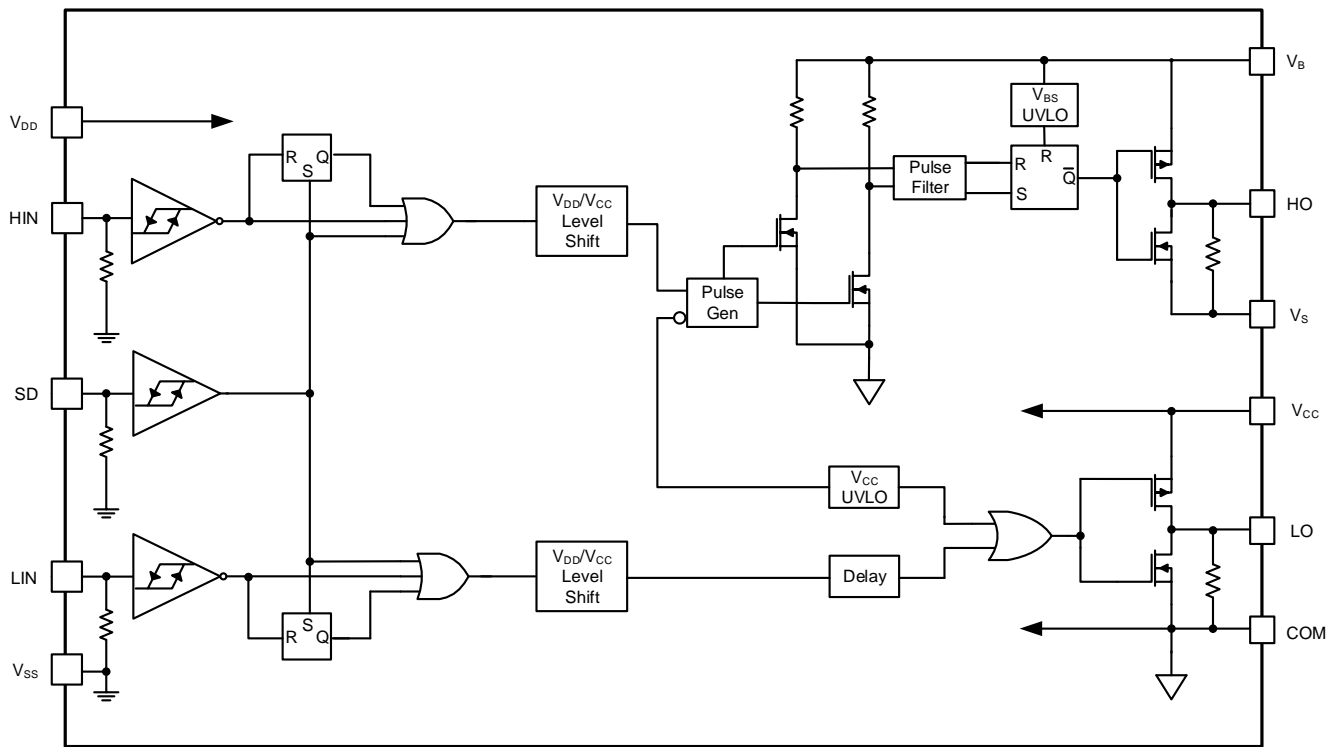
PIN DESCRIPTION

No.	Pin	Description
1	LO	Low-side gate drive output
2	COM	Low-side return
3	V _{CC}	Low-side supply
4	NC	No connection
5	NC	No connection
6	V _S	High-side floating supply return
7	V _B	High-side floating supply
8	HO	High-side gate drive output
9	NC	No connection
10	NC	No connection
11	V _{DD}	Logic supply
12	HIN	Logic input for high-side gate driver output (HO), in phase
13	SD	Logic input for shutdown
14	LIN	Logic input for low-side gate driver output (LO), in phase
15	V _{SS}	Logic ground
16	NC	No connection

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SL2110	SOP16W, Pb-Free	1500/Reel

FUNCTIONAL BLOCK DIAGRAM


ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min.	Max.	Units
V _B	High-side floating absolute voltage	-0.3	625	V
V _S	High-side floating supply offset voltage	V _B - 25	V _B + 0.3	
V _{HO}	High-side floating output voltage	V _S - 0.3	V _B + 0.3	
V _{CC}	Low-side supply voltage	-0.3	25	
V _{DD}	Logic supply voltage	-0.3	V _{SS} + 20	
V _{SS}	Logic supply offset voltage	V _{CC} - 20	V _{CC} + 0.3	
V _{LO}	Low-side output voltage	-0.3	V _{CC} + 0.3	
V _{IN}	Logic input voltage (HIN, LIN, & SD)	V _{SS} - 0.3	V _{DD} + 0.3	
dV _S /dt	Allowable offset supply voltage transient	---	50	V/ns
P _D	Package power dissipation @ T _A ≤ +25°C	---	1.25	W
θ _{JA}	Thermal resistance, junction to ambient	---	100	°C/W
T _J	Junction temperature	---	150	°C
T _S	Storage temperature	-55	150	
T _L	Lead temperature (soldering, 10 seconds)	---	300	

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min.	Max.	Units
V _B	High-side floating absolute voltage	V _S + 10	V _S + 20	V
V _S	High-side floating supply offset voltage		600	
V _{HO}	High-side floating output voltage	V _S	V _B	
V _{CC}	Low-side supply voltage	10	20	
V _{DD}	Logic supply voltage	V _{SS} + 3	V _{SS} + 20	
V _{SS}	Logic supply offset voltage	-5	5	
V _{LO}	Low-side output voltage	0	V _{CC}	
V _{IN}	Logic input voltage (HIN, LIN, & SD)	V _{SS}	V _{DD}	
T _A	Ambient temperature	- 40	125	°C

Note: The input/output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The VS offset rating is tested with all supplies biased at a 15 V differential.

Note: Logic operational for V_S of (COM - 5 V) to (COM + 600V). Logic state held for V_S of (COM-5V) to (COM - V_{BS}).

DYNAMIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15 V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	$V_S = 0$ V	---	140	200	ns
t_{off}	Turn-off propagation delay	$V_S = 0$ V	---	140	200	
t_{sd}	Shutdown propagation delay	$V_S = 0$ V	---	130	160	
t_r	Turn-on rise time		---	15	25	
t_f	Turn-off fall time		---	9	15	
MT	Delay matching, HS & LS turn-on/off		---	---	10	

STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15 V and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} , and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN, and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic "1" input voltage		$V_{DD} \times 80\%$	---	---	V
V_{IL}	Logic "0" input voltage		---	---	$V_{DD} \times 25\%$	
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	$I_O = 2$ mA	---	---	0.2	
V_{OL}	Low level output voltage, V_O		---	0.02	0.15	
I_{LK}	Offset supply leakage current	$V_B = V_S = 600$ V	---	---	50	μ A
I_{QBS}	Quiescent V_{BS} supply current	$V_{IN} = 0$ V	---	65	120	
I_{QCC}	Quiescent V_{CC} supply current		---	300	550	
I_{QDD}	Quiescent V_{DD} supply current		---	0.1	1	
I_{IN+}	Logic "1" input bias current	$V_{IN} = 5$ V	---	8	15	
I_{IN-}	Logic "0" input bias current	$V_{IN} = 0$ V	---	---	5	
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold		7.5	8.9	9.7	V
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold		7.4	8.2	9.4	
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold		7.5	8.9	9.7	V
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold		7.4	8.2	9.4	
I_{O+}	Output high short circuit pulsed current ¹	$V_O = 0$ V, $V_{IN} =$ Logic "1", $PW \leq 10$ μ s	0.8	1		A

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{O-}	Output low short circuit pulsed current ¹	$V_O = 15\text{ V}$, $V_{IN} = \text{Logic "0"}$, $PW \leq 10\ \mu\text{s}$	1.2	1.6		

1) Values are verified by characterization on bench.

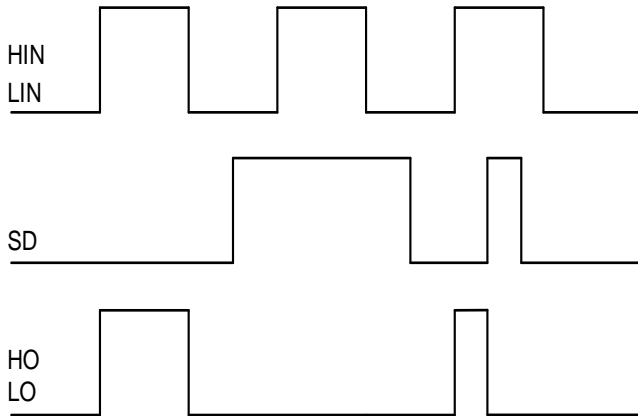


Figure 1. Input/Output Timing Diagram

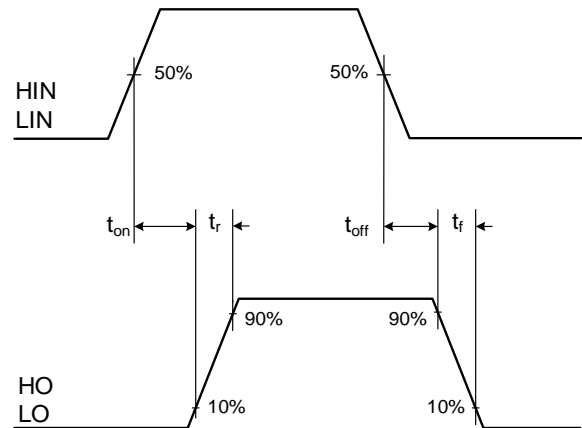


Figure 2. Switching Time Waveform Definition

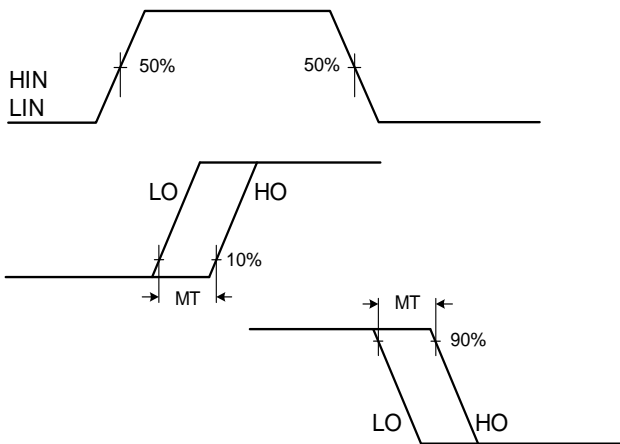


Figure 3. Delay Matching Waveform Definition

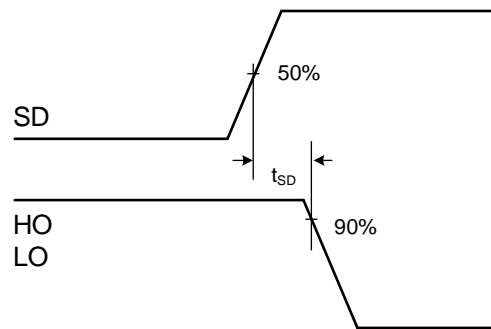


Figure 4. Shutdown Waveform Definition

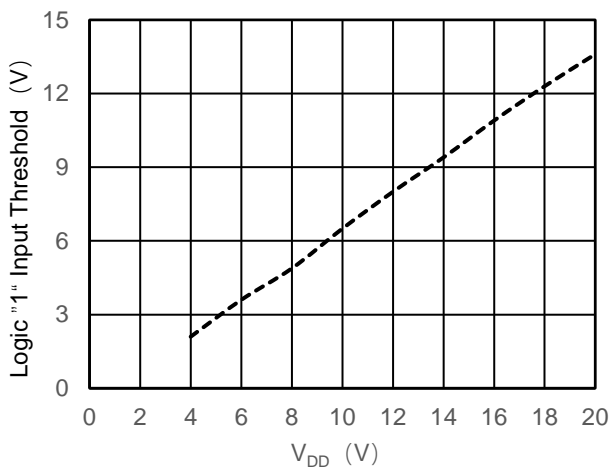


Figure 5. Logic "1" Input Threshold vs. VDD

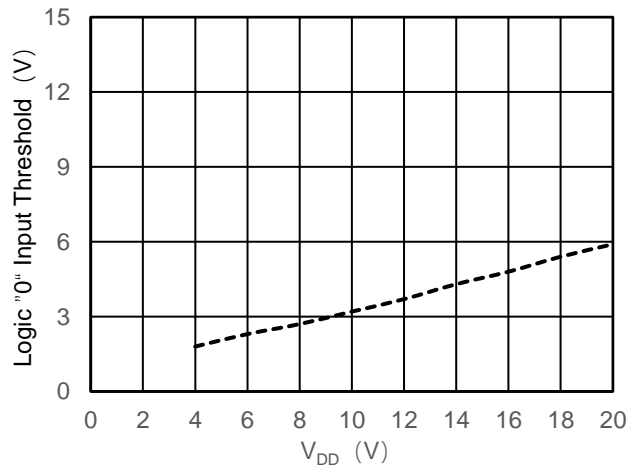


Figure 6. Logic "0" Input Threshold vs. VDD

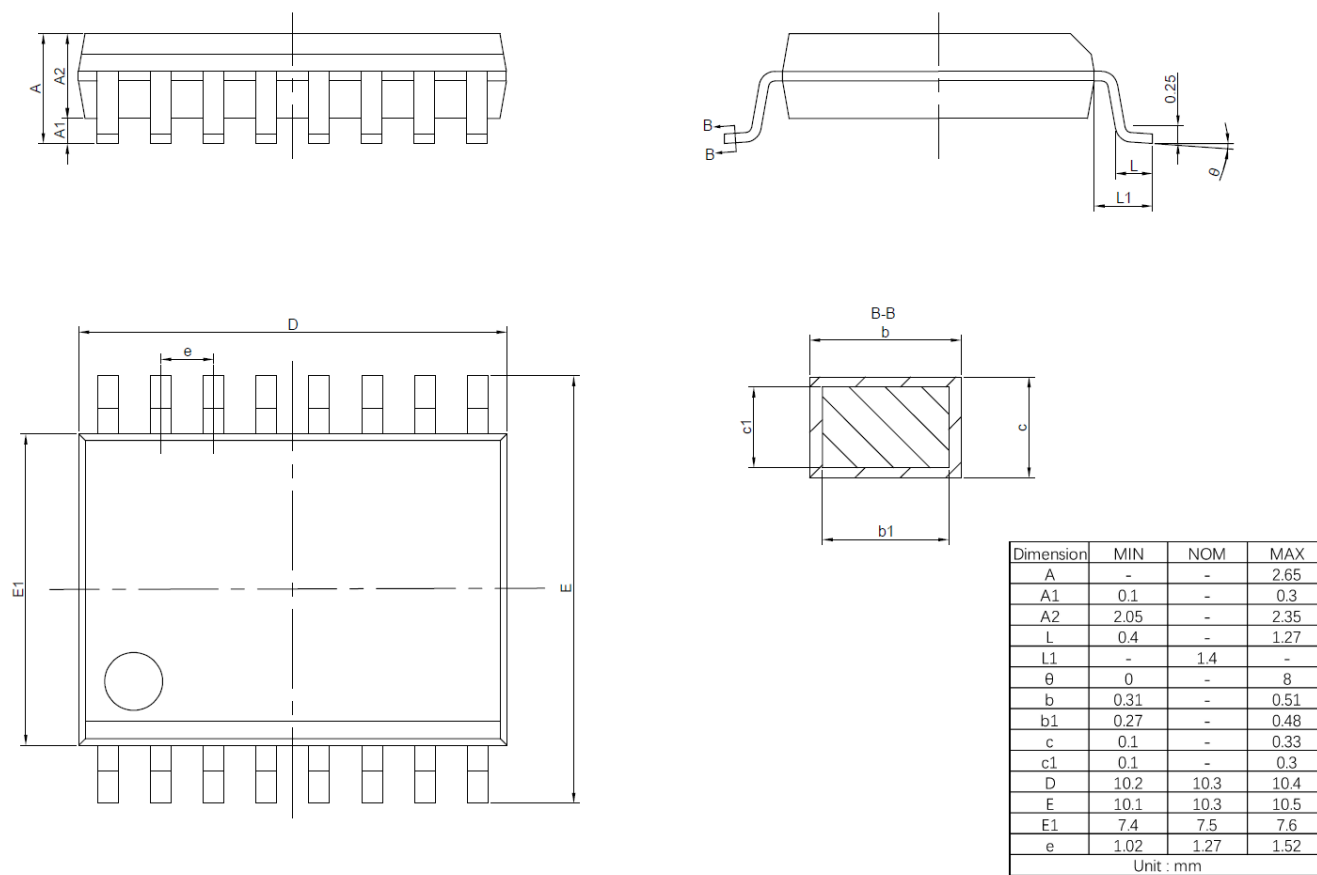
PACKAGE CASE OUTLINES


Figure 7. SOP16W Outline Dimensions